SILICON-EMBEDDED MAGNETIC COMPONENTS FOR ON-CHIP INTEGRATED POWER APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

Xuehong Yu

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
Dec 2014

Copyright © 2014 by Xuehong Yu

SILICON-EMBEDDED MAGNETIC COMPONENTS FOR ON-CHIP INTEGRATED POWER APPLICATIONS

Approved by:

Professor Mark G. Allen, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Albert B. Frazier
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Andrew F. Peterson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Dennis W. Hess
School of Chemical and Biomolecular Engineering
Georgia Institute of Technology

Date Approved: 11 August 2014

DEDICATION

To my parents and my sister for all their support.

ACKNOWLEDGEMENTS

Upon finishing the thesis, I would like to thank many people who have supported me throughout my journey.

First, I would like to express my sincere gratitude to my advisor, Prof. Mark G. Allen, for his leadership, guidance, support and help throughout my PhD study. Dr. Allen allowed me to join the group when I knew little about MEMS/microfabrication and opened the opportunity for me to grow in the field of power electronics and magnetics. I have always been enlightened by his insightful ideas and suggestions when I needed them. What I learned through my PhD study is not only the knowledge about the specific project I worked on, but also the approach to analyze and solve problems in general and the good attitude in dealing with things in life. Dr. Allen set a role model for me and I am very grateful for his patience and dedication on advising me along the way.

I would like to thank my committee members, Prof. Muhannad S. Bakir, Prof. Albert B. Frazier, Prof. Andrew F. Peterson and Prof. Dennis W. Hess, for agreeing to serve on my committee and giving me helpful guidance and suggestions on my work.

I would like to thank Dr. Florian Herrault for his mentorship. I shadowed him to work in the cleanroom when I first joined the group. And later on he gave me enormous guidance and help when we worked on the Arpa-E project. I enjoyed all the discussions and meetings I had with him.

I would like to thank all members in the Microsensors and Microactuators (MS-MA) group at the Georgia Institute of Technology and University of Pennsylvania for their support, discussions, suggestions and friendship. I'd like to thank Mr. Richard

Shafer for all his help in supporting my research and managing our labs.

I would like to thank all members of the Arpa-E powerchip project team from MIT, Dartmouth and UPenn. I have learned a lot, both in and out of my field of expertise, from our biweekly and monthly meetings through teleconference. I enjoyed the collaboration with students/faculties/staff on the project.

Finally, I would like to thank my parents and sister in China for always giving me the love and support needed to accomplish my goals.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of the proposed research is to design, fabricate, characterize and test silicon-embedded magnetic components for on-chip integrated power applications. Driven by the trend towards continued system multi-functionality and miniaturization, MEMS technology can be used to enable fabrication of three-dimensional (3-D) functional devices into the silicon bulk, taking advantage of the 'dead volume' in the substrate and achieving a greater level of miniaturization and integration. As an example, one of the challenges in realizing ultra-compact high-frequency power converters lies in the integration of magnetic components due to their relatively large volume. Embedding 3-D magnetic components within the wafer volume and implementing high-power, through-wafer interconnect for connection to circuitry on the wafer surface is a promising solution for achieving ultra-compact power converters, in which digital control circuitry and power switches are located on the wafer surface, and suitable magnetic components are embedded within the silicon substrate. In order to do this, key tasks in the following areas have been accomplished: development of new fabrication technologies for silicon embedding and 3-D structure realization; creation of high-current, through-wafer interconnects for connection of the device to circuitry; ability to incorporate a variety of magnetic materials when performance enhancement of the device is needed; exploration of a new design space for the devices due to ultra-compactness and silicon interaction; understanding of the complicated loss mechanisms in the embedded devices; and demonstration of device performance and in-circuit operation.

CHAPTER I

INTRODUCTION

There has been continuing desire for increasing complexity and compactness in silicon systems. Increased complexity and compactness has typically been achieved by means of advances in semiconductor manufacturing that lead to larger and larger numbers of transistors to be fabricated on a single chip. As semiconductor technology advances into the nanometer-scale regime, this approach is reaching its limit, necessitating alternative approaches such as chip stacking and system in package (SiP)/system on package(SoP) technologies [17]–[20], where integration of multiple chips or components into a single package is explored for continued system multi-functionality and miniaturization.

However, in many of these approaches, the relatively large volume of the silicon bulk compared to the volume of the active circuitry, even in thinned wafers, remains untapped. To take advantage of this 'dead volume' within the bulk of the silicon wafer, microelectromechanical systems (MEMS) technology can be used to enable integration of three-dimensional (3-D) functional devices into the substrate without consuming valuable die area on the wafer surface or increasing the packaging complexity.

1.1 Statement of the Problem

As an example of technologies that could greatly benefit from embedded 3-D structures, consider high-frequency switched-mode power converters designed for ultra-compactness. By integrating 3-D magnetic components with digital control logic and power electronic switchers on a single silicon chip, these integrated converters can be utilized not only as small stand-alone chargers for portable electronics, but also as

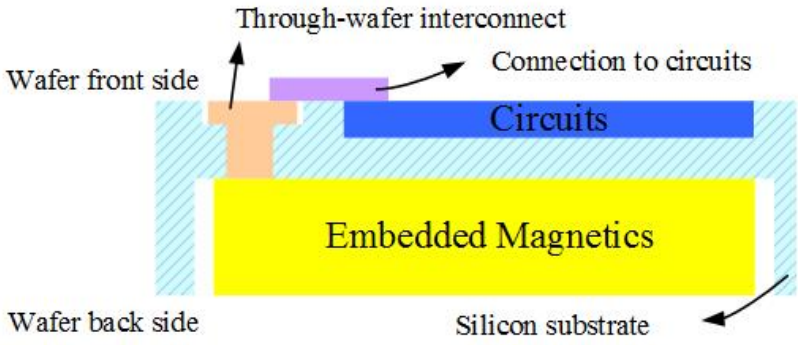


Figure 1: Illustration of a chip-scale integration scheme. A MEMS device is embedded in the wafer volume and connected to the circuitry on the wafer front surface using through-wafer interconnects.

indispensable components of compact electronic systems requiring multiple voltage levels. The increase of the switching frequency of power converters into the megahertz range reduces the required energy storage capability of the magnetic components in these systems and therefore their volume, rendering the integration of microfabricated magnetics on chip possible.

Embedding magnetic components within the wafer volume from the backside and implementing high-power, through-wafer interconnect using MEMS technology for connection to the digital control circuitry and power switches that are located on the wafer surface, as shown in Figure 1, is a promising solution for realizing monolithic ultra-compact power converter systems. This silicon-embedding approach, in comparison to other integration schemes of 3-D structures such as surface-micromachining of the devices on or beside the circuits, offers additional miniaturization and potential performance benefits, which is especially desirable when system profile is a major concern. To realize this concept, a few key tasks in the following areas have to be performed:

1. Development of new advanced fabrication technologies to realize silicon embedding of 3-D structures.

2. Creation of high-current, through-wafer interconnects for connection from the embedded device to circuitry.

3. Ability to incorporate a variety of magnetic materials when performance enhancement of the device is needed.

4. Exploration of new design space for the devices due to ultra-compactness and silicon interaction.

5. Understanding of the complicated loss mechanisms at high frequencies in the embedded devices.

6. Demonstration of device performance and successful in-circuit operation.

1.2 Objectives and Outline

The objective of the proposed research is to design, fabricate, characterize, and test silicon-embedded magnetic components for on-chip integrated power applications. The concept, as discussed before, is to embed magnetic components into the volume of the silicon substrate and implement through-wafer interconnects for connection to the circuitry on the wafer front side. Based on the requirements of DC-DC power converters for driving light-emitting diodes (LEDs), the embedded toroidal inductors have to possess both densely-packed thick windings and deep profiles to achieve high inductances and low resistances within a limited footprint. To achieve it, as listed in the previous section, six key tasks have to be accomplished.

In the remainder of this thesis, the chapters will be organized according to the proposed six tasks. New fabrication technology developed for patterning inside deep silicon trenches to create 3-D toroidal inductors will be introduced first. Processes for incorporating through-wafer, high-power interconnects and integrating magnetic cores into these inductors will then be discussed. Upon understanding the microfabrication constraints, design and optimization strategies for the silicon-embedded inductors are

presented, followed by inductor modeling to understand the losses in the embedded inductors, which helps guide the inductor design and optimization process. Device performance is then demonstrated through characterizations of the fabricated silicon-embedded inductors and successful operation of the inductors in power converter circuits. At the end, preliminary efforts in applying the silicon-embedded components to other applications such as wireless power transfer are also presented.

CHAPTER II

REVIEW OF LITERATURE

With technology development advancing every day, modern electronics never stops evolving towards smaller, thinner and lighter devices while offering more and more functionality. New concepts that may change our way of life continue to emerge, such as motes, a concept brought up recently that is also called smart dust and wireless sensing networks. Having a small, low-cost, low-power computer inside a mote, which connects to the outside world through a radio link, can monitor one or more sensors to gather information of interest. There are potentially many ways to utilize motes. The fundamental idea about motes, though, is the tiny size and the associated tiny cost.

MEMS technology utilizes microfabrication techniques to realize features in the micron and nano scale, and provides miniaturization of various systems, which is essential to many space-constrained applications. In particular, the integration of magnetic components within silicon substrates using MEMS technology offers the potential to create sensors, actuators, and energy conversion devices with high degrees of compactness and functionality.

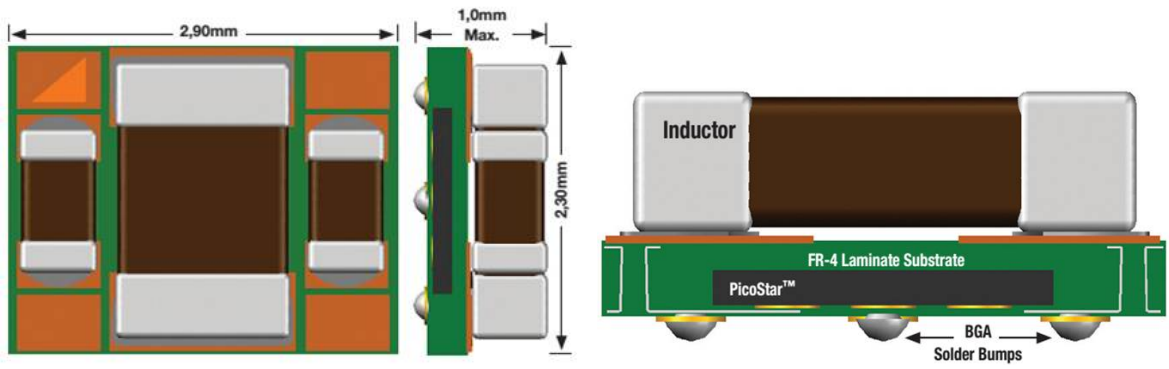
In portable consumer electronics devices with batteries, such as smart phones, computers, tablets and GPS, multiple supply voltages have become very common due to the coexistence of low-power digital circuits, high-speed digital circuits, and analog/RF circuits on a single die, which necessitates the usage of DC-DC power converters. Due to the stringent requirements of miniaturization and integration in these systems, realization of ultra-compact power converters becomes necessary.

2.1 Ultra-Compact Power Converters

DC-DC power converters are used to transform voltages between different levels and comprise an indispensable part of many systems. Buck converters are commonly used as a fundamental power management unit to provide regulated output voltage and current for the loads from a non-regulated battery supply or higher supply rail. Switched-mode inductive converters are the dominant type of DC-DC converters due to their high power density, high efficiency, and excellent transient performance such as line/load regulation. In addition, the recent progression of switched-mode power conversion into the high frequency range reduces the required energy storage of the inductor in the circuit, and consequently the volume of the inductor can be reduced [2], [6], [9], [16], [21]–[25]. This reduced inductor size enables various integration technologies to be developed for realizing ultra-compact power converters with integrated inductors.

The monolithic integration of passive and active components in a DC-DC converter simplifies the external connection complexity, reduces the total footprint and cost, and also introduces additional internal electrical benefits, such as enhancing the efficiency and improving the output voltage regulation. With non-integrated converters that have separate packaged controller chip and external inductors, significant energy is dissipated in the interconnections due to parasitics either on the PCB board or between the components. For application such as power supplies and light-emitting diode (LED) drivers that require large output power, the energy loss due to off-chip power generation and distribution increases significantly, which further reduces the converter efficiency. In addition, delivering power to modules at a higher voltage and converting the voltage down on chip could also scale down the current in the power delivery network [26]. All of these benefits motivate the development of a power converter with higher degree of integration and higher switching frequency.

Currently, research in trying to develop ultra-compact power converters has been



(a) (b)

Figure 2: A MicroSiP^{TM}-enabled power converter device TPS8267xSiP from Texas Instruments: (a) top view, and (b) cross-sectional view [1].

reported. Power-system-in-packaging (PSiP) and power-supply-on-chip (PwrSoC) are the two prevailing approaches in realizing converter miniaturization with integrated passive components. Below are examples of some work that employs various technologies to realize ultra-compact converters.

A series of commercially-available integrated DC-DC step-down converters using MicroSiP^{TM} technology is developed by Texas Instruments for low-power applications [1]. The surface-mount technology (SMT) passive components, including inductors and capacitors, are surface-mounted on top of a chip that is laminated in a FR-4 substrate, as shown in Figure 2. The converter has a size of 2.3 mm x 2.9 mm x 1 mm and operates at 5.5 MHz with an input voltage in the range of 2.3-4.8 V, an output voltage of 1.8 V, a maximum efficiency of 90% and a maximum load current of 600 mA.

Another integrated buck DC-DC converter using SMT air-core inductors is demonstrated with a four-phase topology in [2] for multiprocessors with multiple supply voltages. The inductors were soldered to the pads on the die side of the package, as shown in Figure 3. The converter achieved an efficiency of 80-87% for an output current of 0.3 A, an input voltage of 1.2 V, an output voltage of 0.9 V at an ultra-high

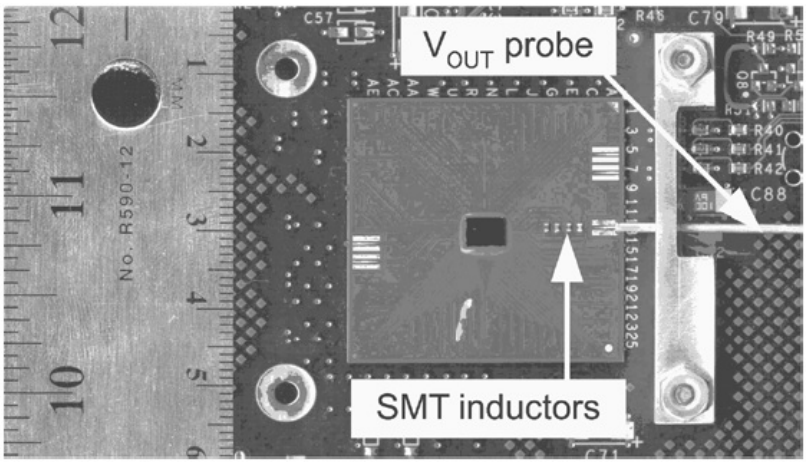
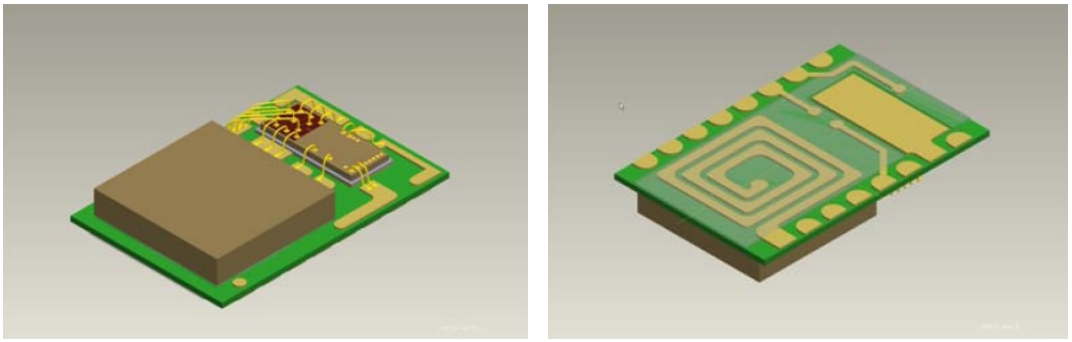


Figure 3: The prototype of the integrated DC-DC buck converter with four air-core inductors mounted on the package [2].

switching frequency of 100 MHz to 317 MHz and occupied an area of 1.28 mm x 0.99 mm under 90-nm CMOS technology.

With printed-circuit-board (PCB) technology, a DC-DC buck converter that monolithically integrates controller and drive circuits, high-speed power MOSFET switches and a spiral inductor is developed by Enpirion, Inc.(now with Altera) [3]. The planar inductor is manufactured on a two-layer PCB substrate with a size of 2.4 mm x 2.4 mm and has a single layer magnetic layer, which contributes to an inductance of 55 nH, as shown in Figure 4. Commercial products of both 12 V and 5 V DC-DC step-down converters are supplied by the company using the developed technology. The 12 V product series has a package size on the order of 10 mm x 10 mm x 3 mm and a peak efficiency of 89%-95% with an output current on the order of a couple of amperes.

A hybrid DC-DC converter was designed and fabricated with a dual spiral sandwiched thin film inductor micromachined on the side of the circuits [4], as shown in Figure 5. The inductor with FeBN magnetic layers (5 mm x 5 mm) measured approximately 1 μH and a quality factor of 4 up to 5 MHz. The buck converter with a size of 15 mm x 12 mm x 1.5 mm achieved an efficiency of 80% at a switching frequency



(a) (b)

Figure 4: Integrated DC-DC buck converter from Enpirion (now with Altera), (a) package assembly with CMOS die, wirebonds, and magnetic die, and (b) bottom metal of the substrate with leads, ground pad, and spiral turns [3].

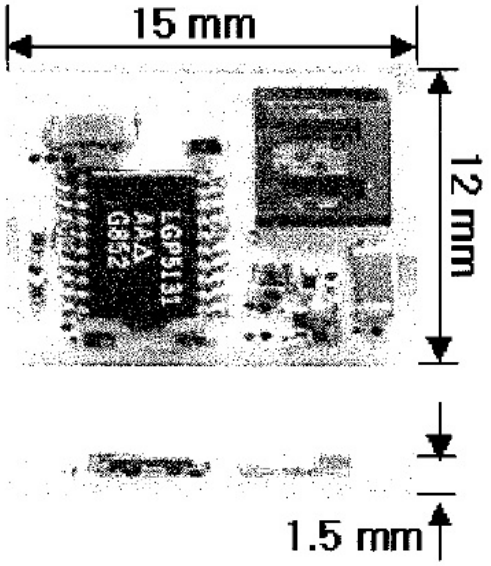
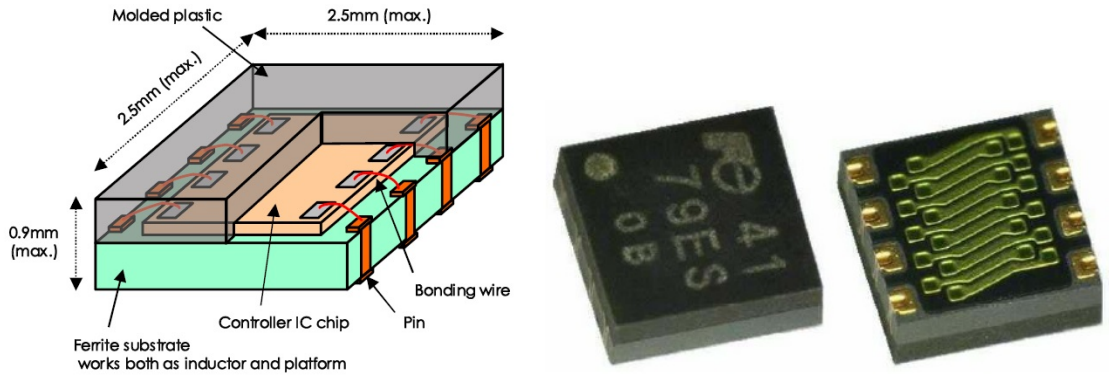


Figure 5: A DC-DC buck converter with a thin film inductor [4].

of 1.8 MHz, an input voltage of 3.6 V, an output voltage of 2.7 V and a maximum power of 1.5 W.

Another ultra-compact buck converter is achieved by mounting an IC chip onto a ferrite substrate where solenoid inductors are formed [27]. The size of the IC chip is 2.9 mm x 2.9 mm x 0.27 mm and the ferrite substrate has a size of 3.5 mm x 3.5 mm x 1.0 mm. At an input voltage of 3.6 V, an output voltage of 3 V, an efficiency of 93.4%

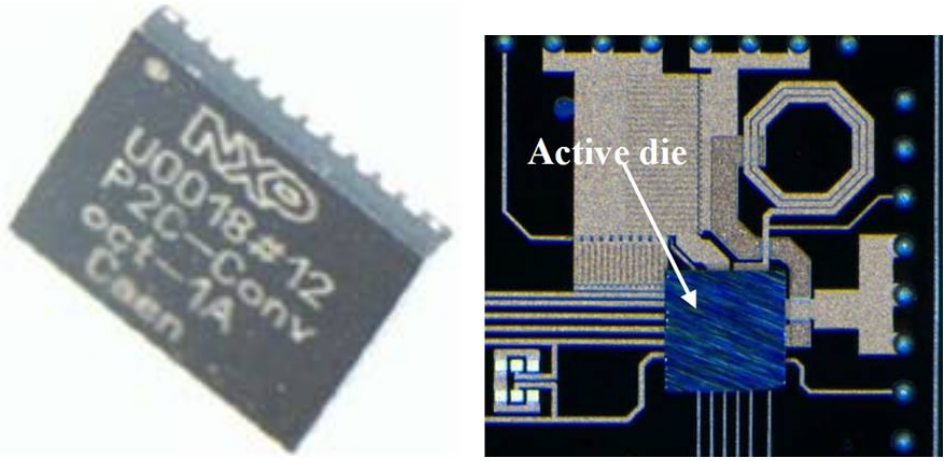


(a) (b)

Figure 6: The integrated boost type DC-DC converter module, (a) the integration structure and (b) the external view of the converter with embedded inductor [5].

is achieved at a switching frequency of 1.8 MHz, an output power of approximately 1 W, and a power density of 81.6 W/cc. The conversion efficiency also decreases with a decreased output voltage. For example, the converter efficiency is less than 85% at an output voltage of 1.5 V with the same circuits. A boost type converter using the same integration approach is later demonstrated with a reduced system profile (2.5 mm x 2.5 mm) in [5], as shown in Figure 6. The converter works at an input voltage range of 2.8 V to 4.5 V, an output voltage of 5 V, a maximum output current of 100 mA and a switching frequency of 2 MHz.

With microfabricated passive components, integration of a step-down DC-DC power converter is achieved using SiP technology [28]. The passive components, including inductors and capacitors, are fabricated on a separate die and flip-chip bonded to the active die where power conversion circuits are. A maximum efficiency of 65% at 80 MHz is achieved for an input voltage of 1.8 V, an output voltage of 1.1 V and an output current of 100 mA. Later, the authors also demonstrated an ultra-compact power converter with the same integration scheme, which exhibits an improved peak efficiency of 87.5% at a switching frequency of 100 MHz and an output power of 85 mW [6], as shown in Figure 7.

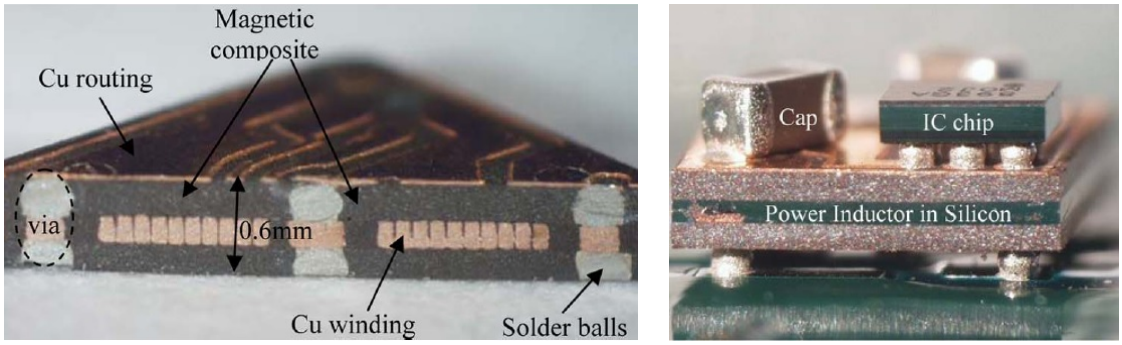


(a) (b)

Figure 7: Integration of microfabricated inductors with an active die using flip-chip bonding [6].

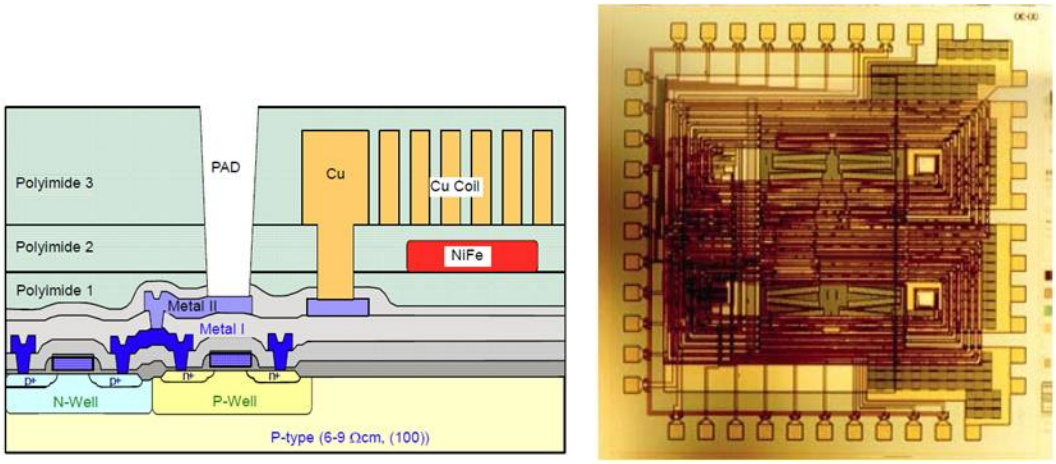
Another ultra-compact buck converter with a microfabricated inductor is demonstrated by surface mounting off-shelf ICs (TPS62601 from Texas Instruments) and capacitors onto a planar inductor that is embedded in silicon with polymer-magnetic power composite deposited on both sides of the silicon [7], as shown in Figure 8. The inductor was measured an inductance of 390 nH and a quality factor of 10 at 6 MHz. The buck converter has a size of 3 mm x 3 mm x 1.2 mm, and delivers 200 mA at an output voltage of 1.8 V with an 80% efficiency at 6 MHz.

With on-chip surface-micromachining technology, a DC-DC converter with monolithically integrated thin-film inductor is demonstrated in [8]. Two spiral thin-film inductors with a bottom layer of NiFe magnetic core are surface-micromachined directly on top of the converter circuits to achieve an on-chip integration of the power converter system, as shown in Figure 9. The area of the thin-film inductor is 3.5 mm x 2.5 mm, while the area of the converter circuits is 4.8 mm x 4.8 mm. An inductance of 0.49 μH and a quality factor of 4.8 at 8 MHz is measured for the micromachined inductor. An efficiency of 72% is obtained for the converter at an input voltage of 3.5 V, an output voltage of 6 V, an output power of 360 mW, and an operating frequency



(a) (b)

Figure 8: Photographs of (a) the cross section of a microfabricated power inductor in silicon (PIiS) and (b) the integrated compact buck converter bonded on testing board [7].

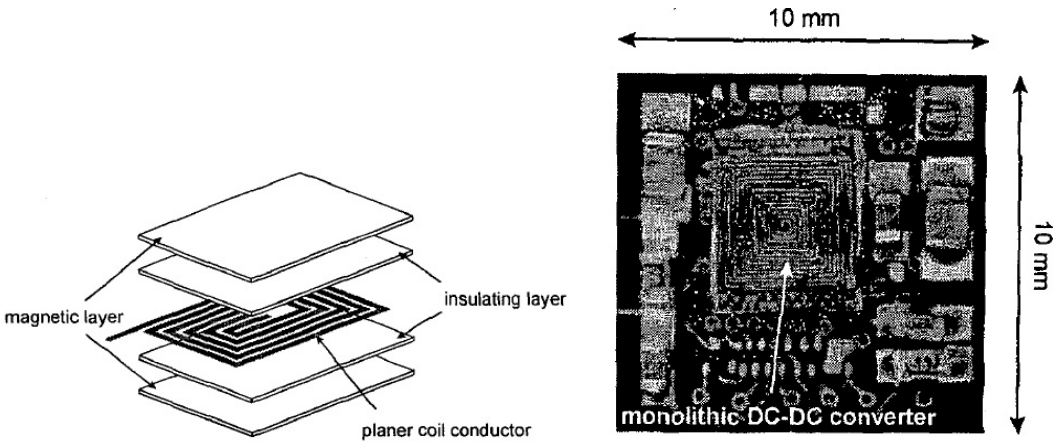


(a) (b)

Figure 9: Integrated planar inductor that is surface-micromachined directly on top of DC-DC converter circuits [8].

of 8 MHz.

Another on-chip integrated DC-DC converter with a thin-film inductor is demonstrated in [9]. The 4 mm x 4 mm thin-film inductor with CoHfTaPd magnetic layers was fabricated by RF sputtering, photosensitive polyimide lithography and electroplating onto the 4 mm x 5 mm power IC, which includes the PWM controller and the MOSFETs, as shown in Figure 10. The monolithic DC-DC converter achieved a



(a) (b)

Figure 10: Integrated planar inductor that are surface-micromachined directly on top of DC-DC converter circuits [9].

Table 1: Recent Work on Ultra-Compact DC-DC Converters

	Sw. freq (MHz)	L (nH)	V_{in} (V)	V_{out} (V)	I_{out} (mA)	η_{max} (%)
[9]	3	960	5	3	300	83.3
[2]	100-317	4*	1.2	0.9	300	80-87
[6]	100	11	1.2	0.85	80.6	87.5
[26]	170	2*2	1.2	0.9	350	77.9
[1]	5.5	n/a	2.3-4.8	1.8	600	90
[3]	20	55	5	1.8	1000	90
[27]	1.8	1650	3.6	3	300	93.4
[7]	6	390	3.6	1.8	200	80
[8]	8	490	3.5	6	60	72
[4]	1.8	1000	3.6	2.7	500	80

maximum efficiency of 83.3% and a power density of 5.6 W/cm^3 at an input voltage of 5 V, an output voltage of 3 V, an output power of 1 W and a switching frequency of 3 MHz.

Although these examples demonstrated ultra-compact power converters using various integration technologies, these converters are targeted at low-voltage low-power applications, which can be seen clearly from Table 1 that summarizes the key information in the discussed work. However, for relatively high-voltage (up to a few

hundred volts) and moderate-power (up to tens of watts) applications such as off-line power supplies, light-emitting diode (LED) drivers, converters and inverters for photovoltaic panels, and battery interface converters, a larger output current, a larger input/output voltage, a larger voltage conversion ratio, and a larger efficiency of usually above 90% is required, which has not been achieved by the published work. Advances in miniaturization and integration of energy-conversion circuitry in this voltage and power range would have a tremendous impact on many applications, and are the interest of our work.

2.2 LED Drivers

Our PowerChip research program, funded by the ARPA-E agency of the US Government, is focused on the development of technologies to radically improve the size, integration and performance of power electronics operating at up to grid-scale voltages (e.g., up to 200V) and moderate power levels (e.g., up to 50 W), with an application demonstrator of a high-efficiency LED driver [16]. Advanced Nitride power devices and device reliability, integrated high-frequency magnetics and magnetic materials, and high-frequency (HF) converter architectures are the key aspects in this program.

LED lighting promises unprecedented reductions in energy consumption, however, the demand for having high-power-density, high-efficiency, and high-power-factor LED drivers has not been met. An investigation of the commercial LED drivers [15], [29] shows that, among a group of commercial line-interfaced LED drivers in the 3-30 W output power range, efficiencies in the range of 64-83% and power factors of 0.59-0.96 are found, with no systems achieving both high efficiency and high power factor. The switching frequencies of these drivers were in the range of 57-104 kHz, with correspondingly low power densities. The sizes of these drivers are dominated by magnetic components due to their low switching frequencies and represents a significant contribution to the overall size of the solid-state lighting system. Substantial

miniaturization of the drivers are achieved through a combination of architecture, circuit topology, and adoption of greatly increased switching frequencies. Although the values of inductors and capacitors vary inversely with the switching frequency, the sizes of passive components do not necessarily decrease monotonically with frequency, owing to magnetic-core loss, voltage breakdown, and heat transfer limits [30]–[32]. Consequently, achieving substantial miniaturization through high-frequency operation further relies upon appropriate passives design and careful selection of circuit topology to minimize the demands placed upon the passive components, especially the magnetic components.

Circuit implementations and controls suitable for power levels of up to a few tens of watts, mid-range input voltages of up to 200 V and LED string voltages in the range of 30-40 V need to be developed. For DC-input applications, an efficient operation across a wide input voltage range (25-200 V) is required.

2.3 Integrated Inductors

Passive components, namely inductors, transformers and capacitors, are often the largest components in power electronics circuits. Although the profile of discrete components with low inductance values have been reduced significantly, such as SMT inductors [33], they usually do not provide a sufficient current driving capability and off-chip connection and parasitics could induce significant losses.

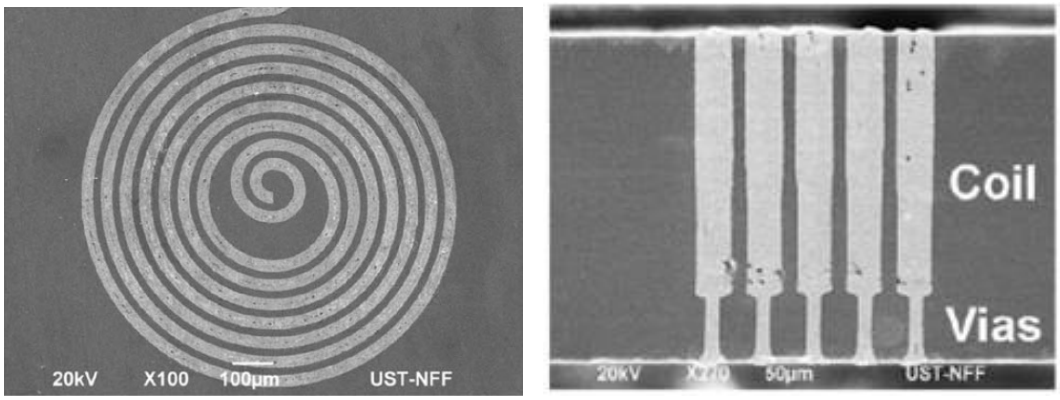
As operating frequencies are increased, the physical size of the passive components can, in theory, be correspondingly reduced, and new fabrication strategies for the magnetics become possible. Realizing this reduction in size requires improvements in magnetics technology. With sufficiently small volume, the magnetics can even be embedded in the substrate of the power circuit or within a secondary substrate and integrated into the same package with the power circuit.

As discussed before in the section of ultra-compact power converters, two main

approaches are used to integrate inductors with the power converter circuits, SiP and PwrSoC technology. SiP technology usually integrates inductor components with silicon chips side by side or on top of each other in the same package [1]–[3], [5]–[7], [27], [34]. Such inductors include SMT inductors [1], [2], inductors in PCB [3], inductors in magnetic substrate [5], [27] and microfabricated inductors on a separate substrate [6], [7], [28]. Although the sizes of these integrated passive components have been reduced greatly, the total thickness of the package using SiP technology is still at least two times that of a silicon chip. Power converters with on-chip integrated magnetic components, although challenging, achieve the ultimate level of system miniaturization as compared to SiP technology [8], [9], [35].

Motivated by this, various microfabrication technologies have been employed to realize air-core and magnetic-core inductors directly on the silicon die [10]–[14], [35]–[40]. For direct integration of inductors on the same substrate as the circuits, the inductors can be surface-micromachined on or beside the active circuits, or embedded into the substrate.

Planar inductors (spiral or racetrack), solenoid inductors and toroidal inductors are the most commonly employed structures for on-chip integration. The advantage of the planar inductor lies in its two-dimensional (2-D) structure that does not require a complex fabrication process. Surface-micromachined air-core planar inductors can be fabricated using one photolithography and sputtering/etching or electroplating process. The magnetic fields created by these geometries, however, are not spatially confined, and can potentially interact with the surrounding lossy materials, which may lead to concerns in ultra-compact designs where components are located closely for miniaturization purposes [3]. Magnetic materials can be deposited around the planar inductor to confine its magnetic field and increase the inductance as well. Yet the development of these materials itself is a non-trivial task and integrating them with the windings complicates the inductor fabrication process significantly [35], [40]. To



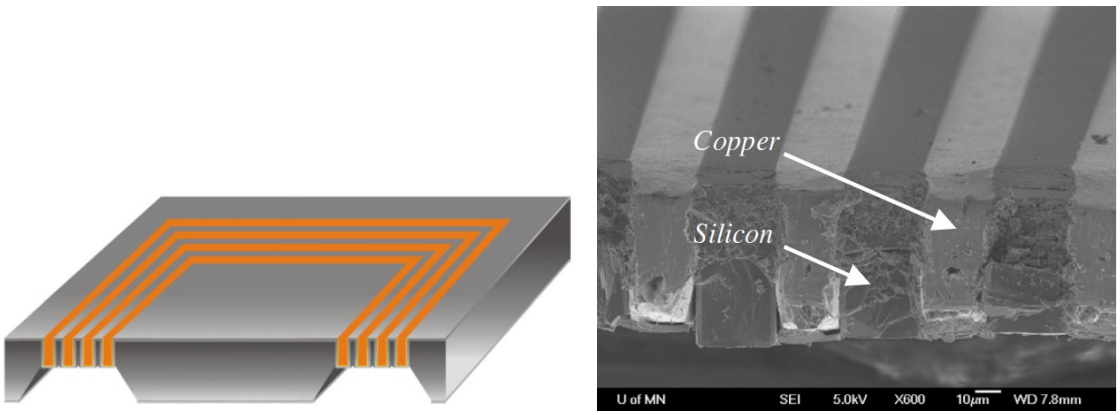
(a) (b)

Figure 11: An embedded planar inductor for on-chip integration [10].

avoid excessive process complication, sometimes planar inductors with only a single-layer magnetic material are surface-micromachined on top of the converter circuits [8], as shown before in Figure 9.

Embedding air-core planar inductors into the silicon substrate has also been demonstrated recently [10], [11], [40], [41]. Figure 11 illustrates a silicon-embedded planar inductor electroplated using a silicon substrate as a mold [10] that has an inductance of 13.1 nH and a quality factor of 3.9 at 100 MHz in an area of 0.8 mm^2. Later the author also demonstrates another embedded planar inductor with an area of 4.5 mm x 4.5 mm, an inductance of 4 μH and a peak quality factor of 19.6 at 2.5 MHz [41]. To improve the inductor performance, the bottom silicon layer under the planar windings can be selectively removed [11], as shown in Figure 12. A high quality factor of over 60 at 30-40 MHz was consequently measured with an inductance of 2 μH for the embedded inductor. However, these planar inductors, as discussed before, might cause interference problems in ultra-compact power converter systems.

Solenoid and toroidal inductors require more complex fabrication techniques due



(a) (b)

Figure 12: An embedded planar inductor with silicon partially removed under the winding area, (a) schematic view, and (b) cross-sectional view of the fabricated inductor [11].

to their 3-D structures [12]–[14], [36]–[39], however, they offer some distinct advantages. Toroidal inductors constrain the magnetic flux within a closed path in contrast to the substrate-penetrating magnetic field that planar inductors generate, and therefore can mitigate the magnetic interference problem with surrounding objects and complex shielding techniques can be bypassed. This flux containment offered by toroidal inductors may be of special importance for ultra-compact converters, in which the physical separation of components is minimized. In addition, various well-developed magnetic cores can be readily integrated with solenoid/toroidal inductors using different techniques without complicating the process significantly [14], [37], [42].

Previous efforts to embed solenoid/toroidal inductors within the volume of silicon substrates have also been reported [12]–[14], [43]. A silicon-embedded RF solenoid inductor with suspended aluminum windings is demonstrated in [12] using a concise process technology without employing lithography process on sidewall and trench-bottom patterning, as shown in Figure 13. Inductances of 2.2 nH, 3.3 nH and 3.6 nH are measured with quality factors of 23.7, 17.8 and 14.4, respectively, at approximately

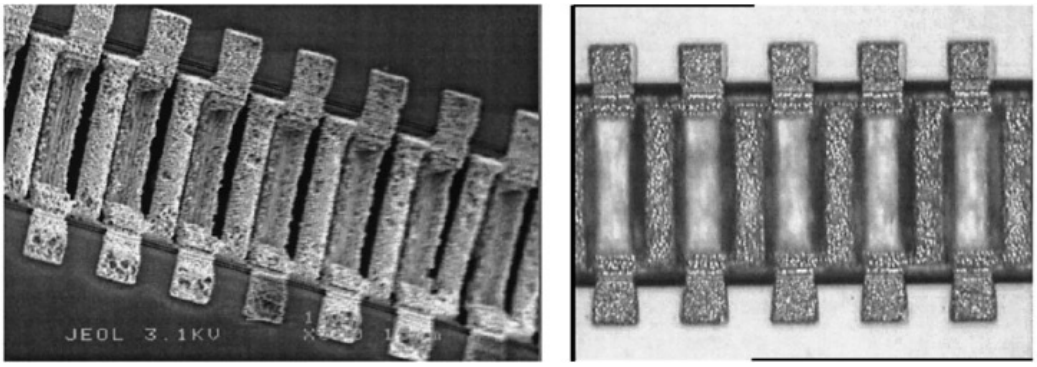
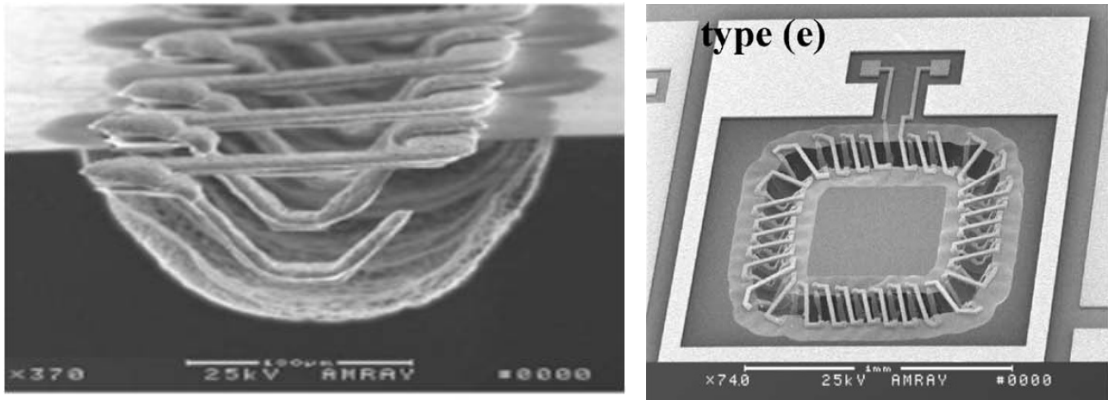


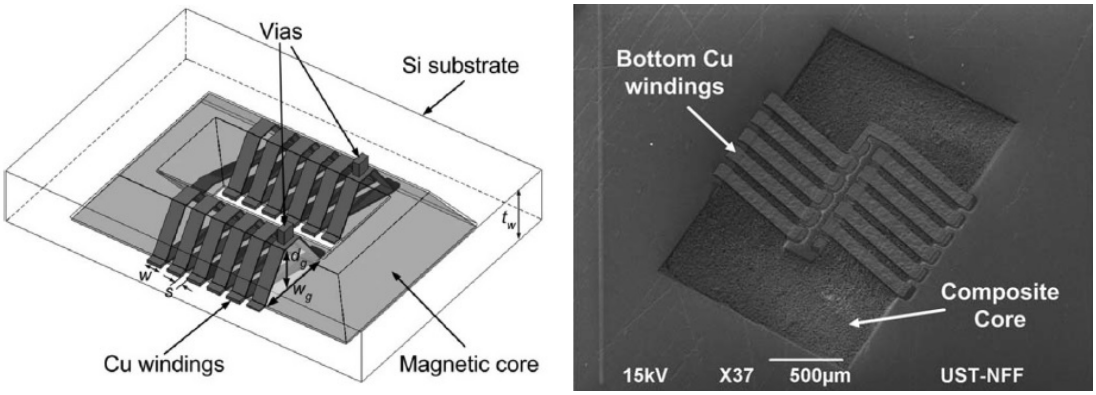
Figure 13: A silicon-embedded solenoid inductor with suspended windings [12].



(a) (b)

Figure 14: Embedded toroidal inductors with suspended windings, (a) solenoid inductor, and (b) toroidal inductor [13].

4.5 GHz. Figure 14 shows an air-core embedded toroidal inductor fabricated in a silicon cavity with suspended windings using anisotropic silicon etching and spray coated photoresist for conductor patterning [13]. The toroidal design with the largest inductance exhibits an inductance of 9.06 nH and a peak quality factor of 17.8 at 3.1 GHz. Figure 15 illustrates a silicon-embedded toroidal inductor with an integrated MnZn ferrite composite core [14]. An inductance of 43.6 nH and a peak quality factor of 16.2 is achieved by the 2.9-mm^2 inductor. An embedded toroidal inductor with a laminated NiFe core is also developed in a footprint of 5.6 mm x 5.6 mm in [43]. The inductor exhibited an inductance of 500 nH for up to 10 MHz, a DC resistance of 95



(a) (b)

Figure 15: Silicon-embedded toroidal inductors with magnetic core, (a) schematic view, and (b) a SEM image of the fabricated inductor [14].

Table 2: Comparison of the measured inductances and quality factors of various silicon-embedded inductors

Reported work	Type	L(nH)	Qmax@freq
Fang [14]	Toroid	43	16@60 MHz
Liang [12]	Solenoid	3.3	17.8@4.5 GHz
Gu [13]	Toroid	9.06	17.8@3.3 GHz
Wu [10]	Planar	15.8	5.5@16 MHz
Pan [11]	Planar	2000	60@30 MHz

$m\Omega$ and a maximum quality factor of approximate 20 at 2 MHz.

In general, these solenoid/toroidal inductors possessed a shallow profile and sparse windings due to fabrication limitations and therefore achieved mostly low inductance values that were only suitable for RF application, as summarized in Table 2. When considering the next-generation power converter systems with operating frequencies of 10-100 MHz, high inductance and substantial conductor thickness in excess of those achievable by RF inductors is required. These goals dictate embedded toroidal inductors with deep profiles (on the order of hundreds of micrometers), dense windings, thick conductors and integrated magnetic materials if needed, which suggests that fundamental advances in fabrication technologies would have to be made to enable patterning in deep trenches to generate these structures.

2.4 Patterning on Non-Planar Surfaces

Since embedding structures inside silicon requires patterning in deep silicon trenches, which dictates non-planar fabrication technologies that are significantly different than patterning on planar surfaces, a discussion of the reported non-planar fabrication techniques is presented in this section.

Generally, two techniques have been demonstrated to be capable of patterning on 3-D recessed surfaces: a spray-coating technique with proximity lithography, and a shadow mask method. The spray-coating of photoresist has been well-studied and reported to generate defined features in etched silicon trenches [13], [44], [45]. However, to enable pattern definition on the trench sidewall, the trenches would have to be formed with slanted sidewalls, which could result in a trench opening seven times larger than the trench bottom , which obviously increases the footprint of the device [13].

Shadow masking can also be used for patterning in trenches. Traditional shadow masks are 2-D planar structures that are aligned and attached to the device wafers to define metal patterns during evaporation [46], [47]. This approach is challenging for deeply recessed surfaces because of the pattern blurring introduced due to the gap that exists between the planar shadow mask and the recess. Recently, 3-D shadow masks that possess self-aligning mechanical structures have been demonstrated to enable fine feature patterning in deep recessed surfaces [48]–[50]. However, the deposited metal layer is not uniform across the non-planar surfaces, and the margins between the drop-in mask and the trench sidewalls do not favor the use of conformal deposition methods such as sputtering when sidewall coating is needed. For sidewall patterning, the directional evaporation method required multiple sample tilts during deposition [49], which exacerbates the pattern blurring problem due to multiple depositions. Thus, there is a continuing need to further develop patterning technologies on non-planar surfaces for device embedding applications.

CHAPTER III

SILICON EMBEDDING TECHNOLOGIES

The silicon-embedding approach has found applications in integrating many MEMS devices and structures such as accelerometers [51], [52], microgenerators [53], interconnects and copper circuitry [44], [46], magnetic components [10]–[13], [54], Hall sensors [47], and microfluidic devices [48].

To date, most of the published research has focused in embedding two-dimensional (2-D) structures into a silicon substrate due to their less complex geometry and ease in fabrication process [10], [11], [44], [46]. Significant challenges remain in embedding complex three-dimensional (3-D) structures with deep profile into the silicon. Creation of devices directly inside the silicon trenches with batch-fabrication-compatible technology, although challenging, needs to be addressed.

In this chapter, two different approaches for embedding 3-D toroidal inductors into deep silicon trenches with vertical sidewalls are first presented, based on the development of a lithography-based technique and a shadow-mask technique respectively. Then, processes for incorporating through-wafer interconnects into the embedded inductors is introduced to realize connection from the device to circuitry on the wafer surface. To further enhance the inductor performance, magnetic cores can be integrated into the toroidal inductors using a drop-in approach, which is compatible with both of the aforementioned embedding technologies. In addition, based on the shadow-mask approach, a creative process for implementing double-layer winding structures into the embedded inductors is also developed, overcoming the fabrication constraints and boosting the inductance within the limited footprint. At the end, a discussion about the developed processes is presented.

3.1 Lithography-Based Approach

The lithography-based approach combines a spray-coating technique with thick epoxy patterning and dry-film lithography on non-planar surfaces to enable creation of complex 3-D structures in deep silicon trenches. A schematic of the embedded inductor design resulting from this approach is shown in Figure 16. Conductors are defined in the etched trench using spray coating and fine proximity lithography. Patterning on the vertical sidewalls is avoided by processing thick SU-8 to form a mold for electroplating the vertical conductors. An air gap must be maintained between the SU-8 mold and the sidewall to facilitate seed layer removal, which isolates the device at the end of the fabrication process. The complete process flow for realizing the embedded inductor is shown in Figure 17. The through-wafer interconnects are temporarily ignored in the process here as they will be introduced later. For better illustration, the silicon wafer is drawn upside down throughout the entire process, and the front and back side of the wafer will be referred to as indicated in Figure 17.

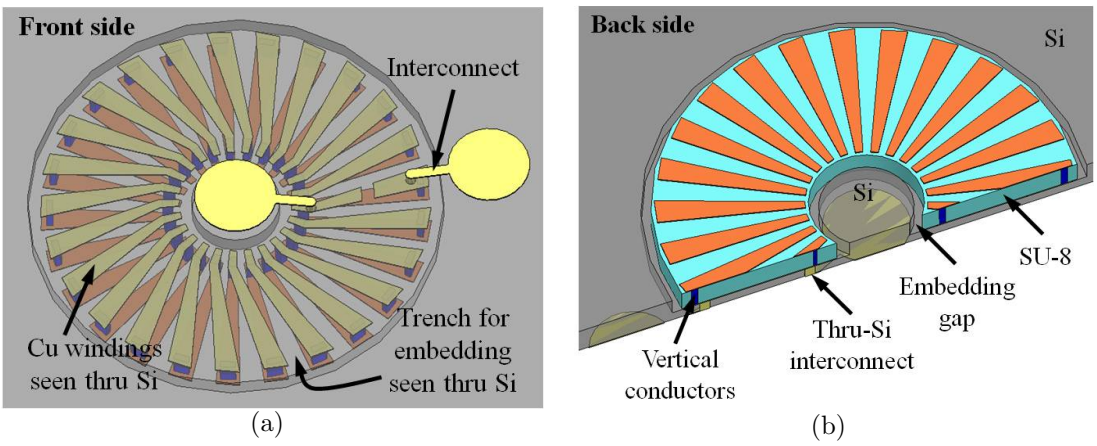


Figure 16: Schematic of the embedded 3-D toroidal inductor using lithography-based approach: (a) wafer front side with silicon substrate drawn partially transparent and SU-8 epoxy removed to illustrate the embedded structures; and (b) wafer back side with cross-sectional cut.

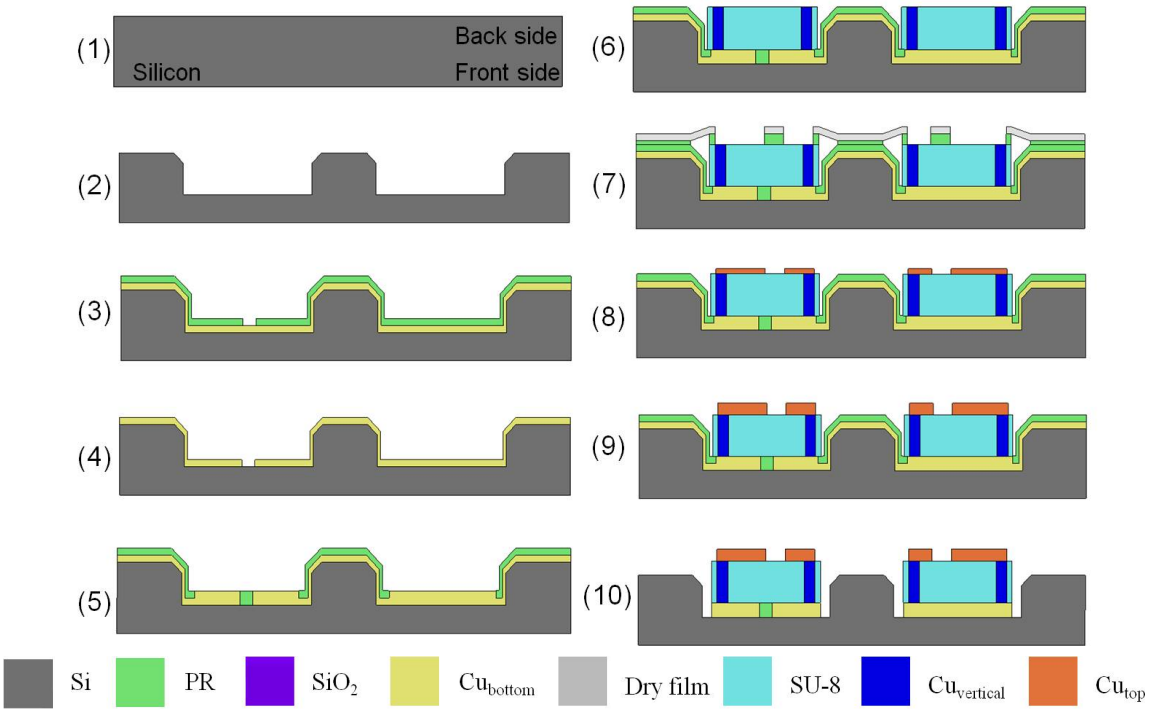


Figure 17: Fabrication process of the toridal inductor using the lithography-based silicon-embedding approach.

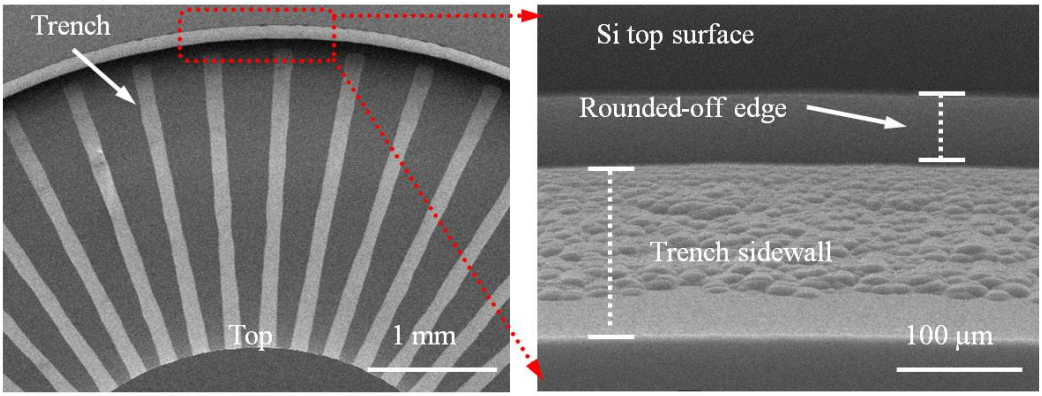


Figure 18: Patterned seed layer in silicon trench with rounded-off edges in step (2).

Referring to Figure 17, fabrication begins with a standard 4-inch silicon wafer in step (1), whose thickness is 500 μm and resistivity is in the range of 1-30 $\Omega \cdot cm$. A silicon trench of 300 μm depth and 2 mm width is first etched into the back side of the wafer through the Bosch inductively coupled plasma process as shown in step (2). A cavity-shaping technique is utilized to form rounded-off edges during

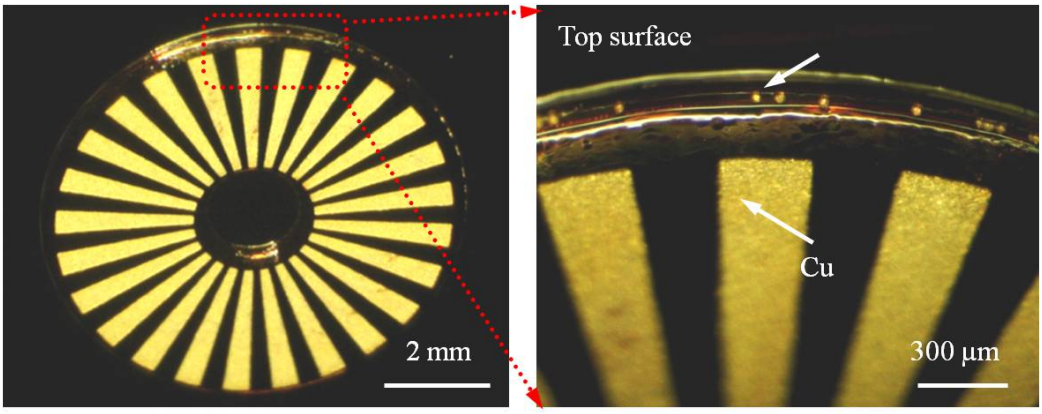


Figure 19: Electroplated bottom copper conductors in the trench in step (5).

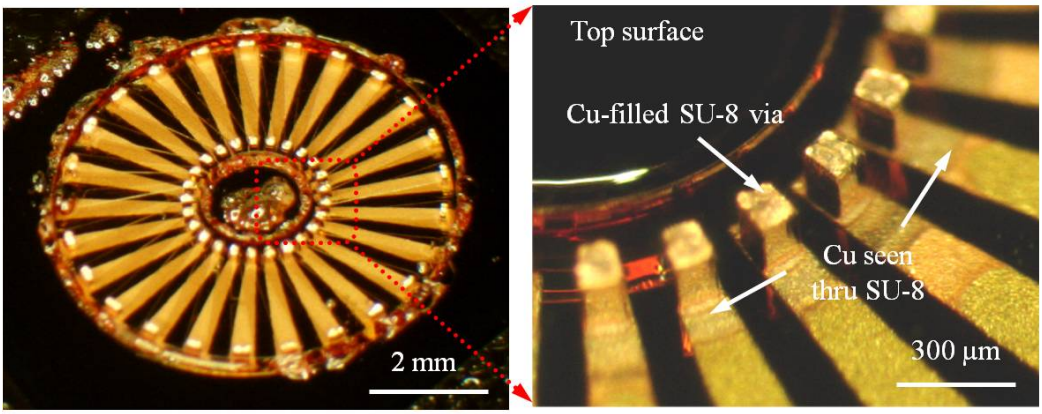


Figure 20: Electroplated vertical copper conductors with SU-8 mold (transparent) in step (6).

the etching to facilitate uniform coverage of spray-coated photoresist on the edges. After deposition of PECVD oxide as an insulation layer and metal sputtering, spray coating of photoresist, proximity lithography and wet etching is performed to obtain a patterned seed layer for radial windings on the recessed bottom surface of the trench as shown in steps (3) and (4). With a spray-coated photoresist mold defined again in step (5) to protect the metalized trench sidewalls and wafer surface, radial copper windings are then electroplated. After hard baking the photoresist, thick SU-8 is cast and patterned in the trench, followed by electroplating to form the vertical conductors

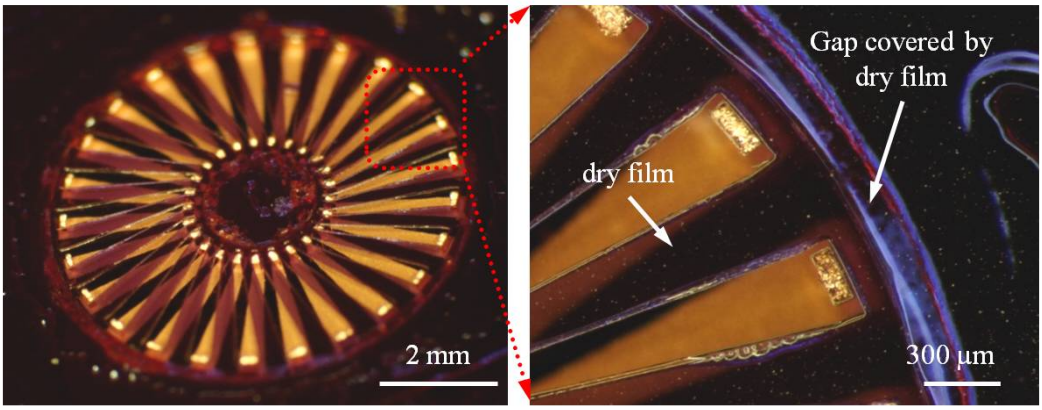


Figure 21: Laminated and patterned dry-film photoresist in step (7).

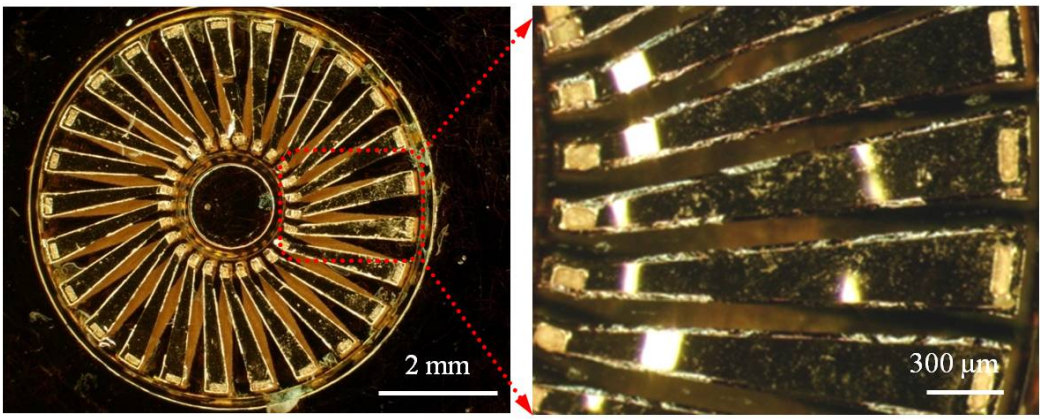


Figure 22: Patterned seed layer after lift-off of dry film in step (8).

in step (6). In this step, good wetting of the SU-8 vias prior to electroplating is the key to ensure high-quality bottom-up filling of the vias because air bubbles tend to be trapped in the vias due to the high aspect ratios of these vias and the surface hydrophobicity of the cross-linked SU-8. Surface treatment and vacuuming can help to remove the bubbles and facilitate the electroplating process. To fabricate the radial conductors on top of the SU-8 mold, a laminated dry-film technique is employed to generate a patterned seed layer through a lift-off process on the complex 3-D surfaces, as shown in steps (7) and (8). The dry film prevents the gap between the SU-8 mold and the silicon substrate from being sputter-coated, which would otherwise be

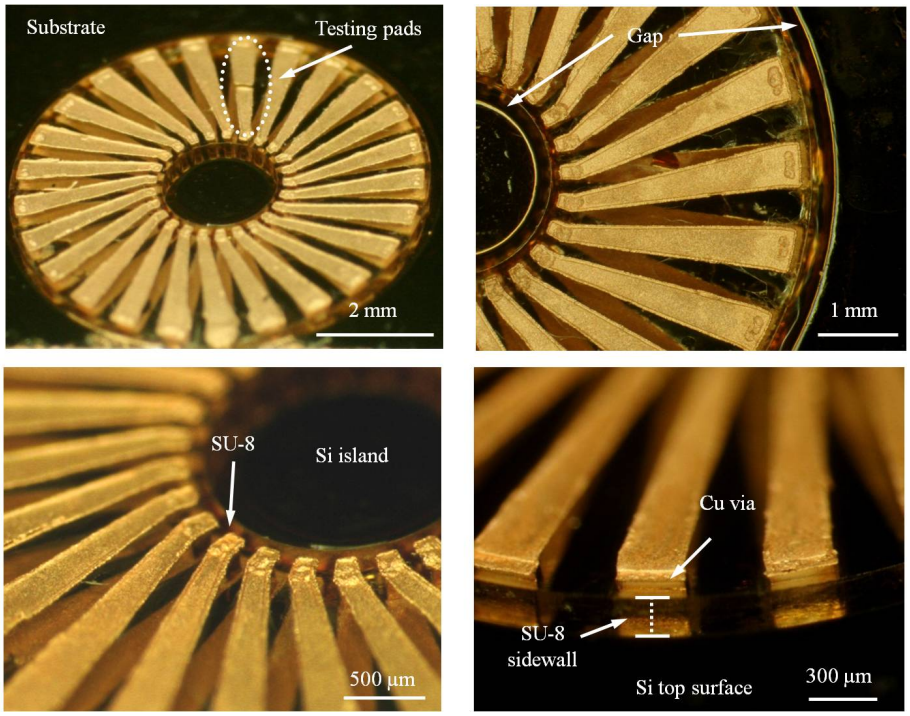


Figure 23: The fabricated inductor embedded in silicon using the lithography-based approach.

challenging to remove due to the nature of the narrow gap. An additional layer of patterned photoresist under the dry film, as shown in step (7), can facilitate clean removal of the dry film in acetone. The top radial conductors are then formed by electroplating in step (9) and the device is completed after removing the hard-baked photoresist layer using oxygen plasma and etching away the underlying seed layer in step (10).

Scanning Electron Microscopy (SEM) images and optical photomicrographs of the partially-fabricated devices are presented for selected steps in Figure 18, 19, 20, 21, 22 and a completed inductor with 25 turns is shown in Figure 23 with electrical testing pads located on one radial conductor that is intentionally separated into two pieces. The minimum gap between two adjacent copper conductors in the inner diameter of the inductor is approximately 120 μm and the vertical conductors buried in SU-8 at the inner diameter are approximately 125 μm by 160 μm. The inductor top surface

is approximately 100 μm higher than the silicon surface due to the fact that SU-8 has to be cast thicker to enable reflowing and planarization across the substrate during soft baking steps.

3.2 3-D Shadow-Mask Approach

The shadow-mask approach utilizes a specially-designed 3-D silicon shadow mask that is formed through multilevel wafer etching to realize direct patterning of the metal layer on both the vertical sidewall and the bottom surface of the deep trench simultaneously. Moldless electroplating can then follow to form the copper conductors along the entire vertical sidewall and the bottom surface of the trench simultaneously. The overall processing time of the shadow-mask approach is significantly reduced compared with the lithography-based approach due to the elimination of several lithography steps, thick epoxy processing steps and the lengthy via-filling step. A schematic of the inductor structure resulting from this approach is shown in Figure 24, which possesses a slightly different geometry than in the lithography-based approach. For

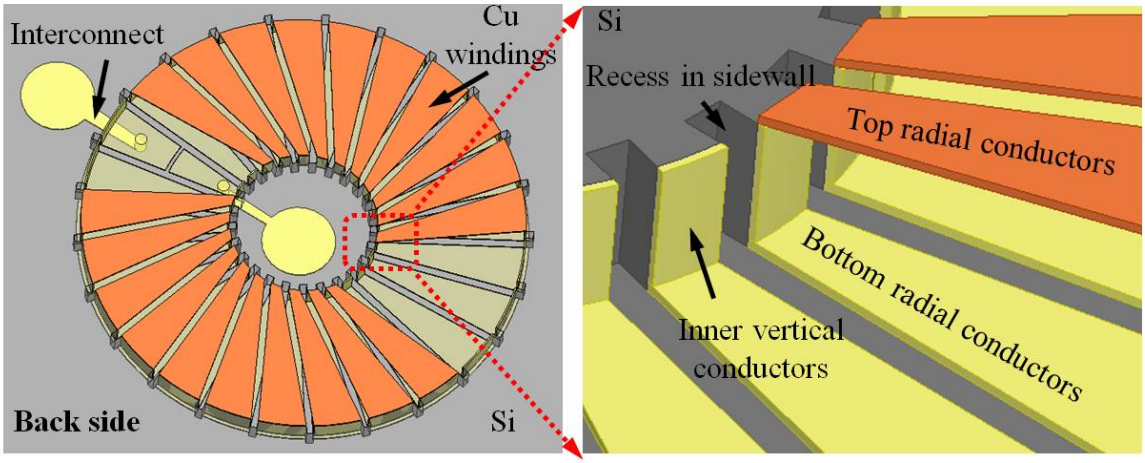


Figure 24: Schematic of the embedded 3-D toroidal inductor using the 3-D shadow mask-based approach: bottom view of wafer back side. Some radical conductors are removed for illustration, and silicon substrate is drawn partially transparent to show the through-wafer interconnects on the front surface of the wafer.

example, the vertical conductors sit directly on the passivated sidewalls of the silicon trench with no air gap introduced between them. These conductors are isolated from each other by the recesses etched into the vertical trench sidewalls. The upper surface of the fabricated inductor is maintained coplanar with the backside surface of the wafer.

The fabrication process of the shadow-mask approach proceeds in two parts. First, the 3-D silicon shadow mask is designed and fabricated; then, the 3-D shadow mask is applied to the inductor fabrication. It should be noted that the shadow mask, once fabricated, can be reused.

To enable conductors to be formed on the vertical sidewalls of the silicon trench directly, a conformal metal deposition method (sputtering) has to be used in order to obtain a uniform seed layer on all exposed areas (bottom and side) of the deep trench. However, sputtering could introduce severe pattern blurring due to the non-directional characteristic of the sputtered metals and the intrinsic margins that exist for registering and inserting the shadow mask into the device wafer. Therefore, special features on the shadow masks and device wafers have to be designed to ensure clean pattern definition through metal layer sputtering.

The design and registration schematic of the shadow mask is illustrated in Figure 25. The multiple spoke-like structures, when looking at the bottom side of the shadow mask, as shown in Figure 25(a), are designed to fit into the silicon trench and define the spacings between adjacent copper conductors during metal sputtering. The protruding ends on the spokes, as seen from the magnified views, are designed to fit into the recesses that have been etched into the vertical sidewalls of the silicon trench, achieving self-isolation of the conductors to be fabricated on the vertical sidewalls. The underlying mechanism, as shown in Figure 25(b), is that the tortuous path between regions 1 and 2 prevents the sputtered metals from entering the recess, keeping region 2 free of any metal deposition, and therefore ensuring isolation between the

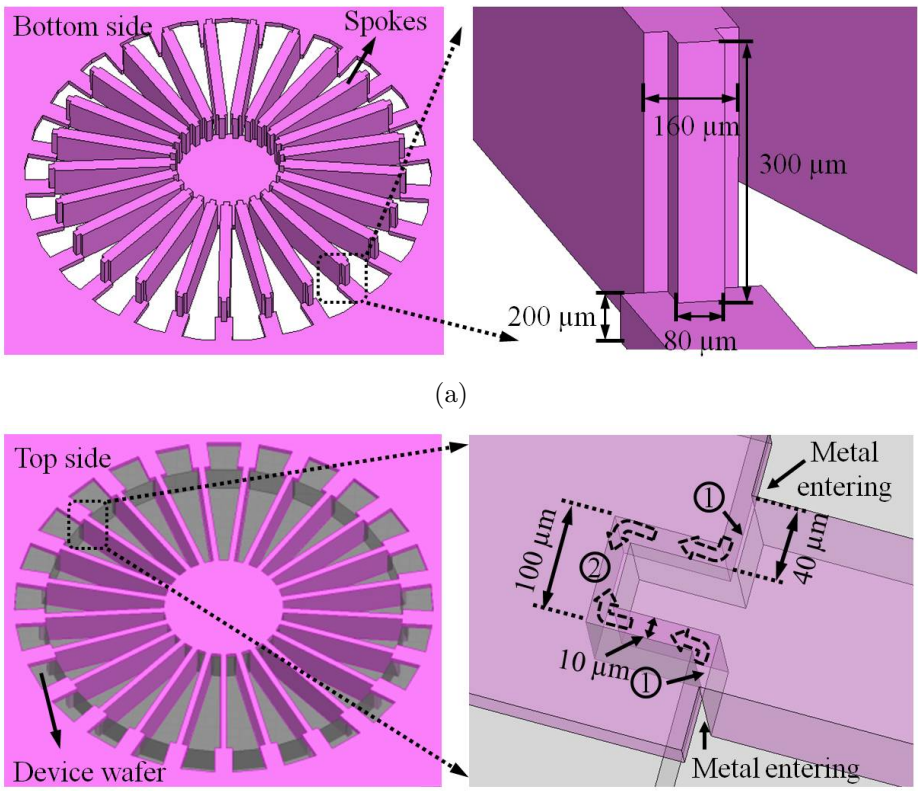


Figure 25: Schematic of the designed 3-D shadow mask: (a) bottom view of the mask with details of the 3-D spoke structure, (b) top view of the mask after insertion into the device wafer with magnified view of the registration scheme. The portion of the shadow mask that covers regions 1 and 2 in the magnified view of (b) is drawn partially transparent for illustration.

to-be-formed vertical conductors on the trench sidewalls. In addition, the protruding ends on the spokes also act as alignment marks during registration and insertion of the shadow mask into the device wafer.

The detailed process for fabricating the 3-D silicon shadow mask is shown in Figure 26. Starting with a standard 4-inch wafer that is 500 μm thick in step (1), a double-layer mask consisting of oxide and photoresist are first formed through wet etching and photolithography in step (2). The photoresist mask is used for etching 200 μm silicon into the wafer through Bosch process, as shown in step (4), which defines the thickness of the connection framework in the shadow mask, and the oxide

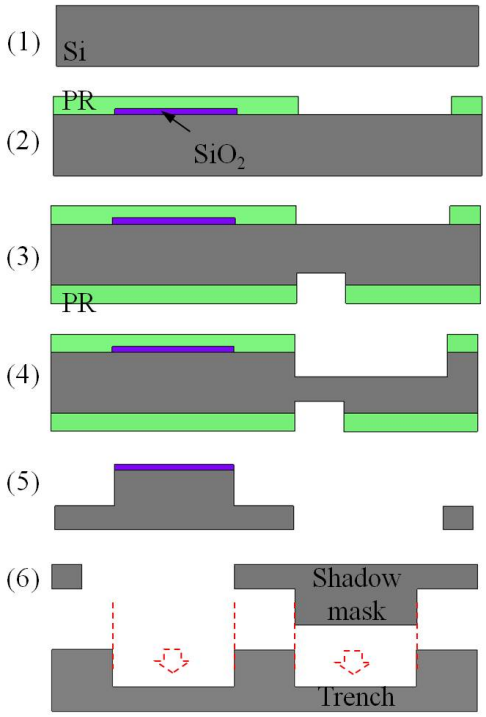


Figure 26: Fabrication process of the 3-D silicon shadow mask.

mask is used to etch 300 μm silicon to form the spokes as well as the open area in the mask that allows metal to be deposited through, as shown in step (5). An additional shallow etching step is conducted in step (3) prior to the etchings in step (4) and (5) in order to compensate for the lower etching rate of small patterns at the inner diameter of the inductor, which is due to Deep Reactive Ion Etching (DRIE) lag. This shallow etching step is critical as non-uniformity-based over-etching of the spokes and framework may result in overly fragile structures. At the end, after stripping the oxide in step (6), the silicon shadow mask is ready for use. SEM images of the fabricated 3-D silicon shadow masks are shown in Figure 27.

Once the shadow mask has been fabricated, inductor fabrication can commence. The complete process flow for fabricating the embedded inductors using the pre-manufactured shadow mask is illustrated in Figure 28. The cut line to show the cross section of the inductor in the process flow is assumed to go through one bottom

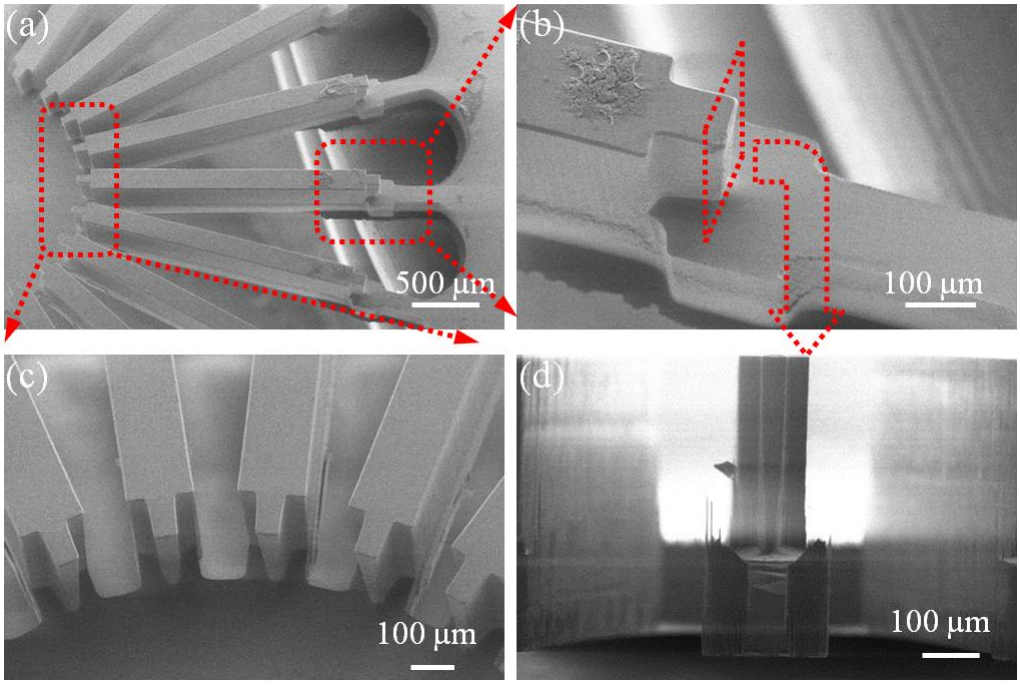


Figure 27: SEM images of the fabricated 3-D silicon shadow mask: (a)-(c) tilted-view and (d) side-view of the spoke structure.

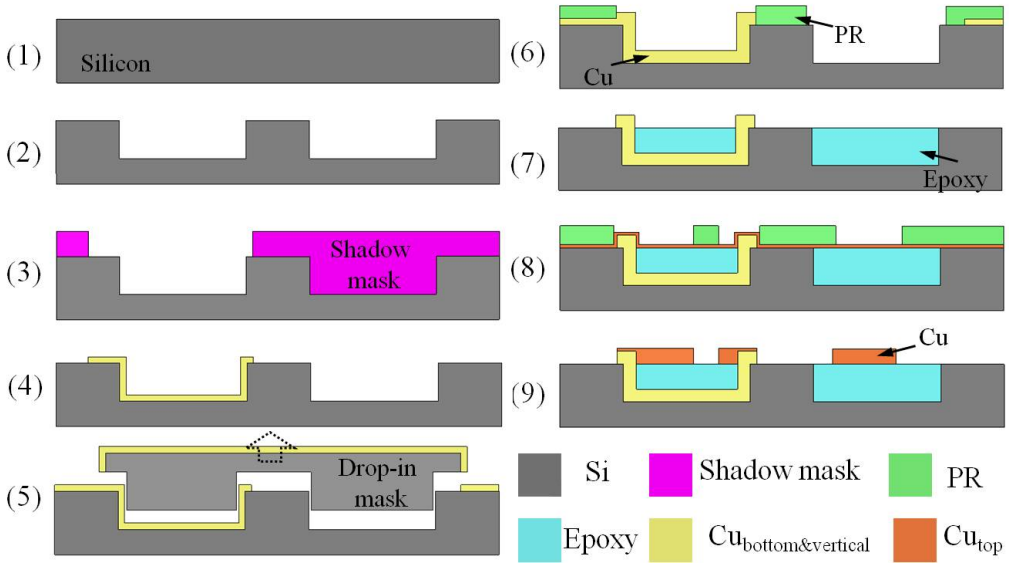


Figure 28: Fabrication process of the embedded toroidal inductors using the 3-D shadow mask-based approach. Features are not drawn to scale.

winding in the left trench and the gap area between two adjacent windings in the right trench. Therefore, all the drawings are completed based on this assumption.

Starting with a standard 4-inch wafer that has a thickness of 500 μm and a resistivity in the range of 1-30 $\Omega \cdot cm$ in step (1), a silicon trench with vertical sidewalls and recesses into the sidewalls is first formed using Bosch etching process as shown in step (2). After deposition of a passivation layer such as PECVD silicon dioxide, the pre-fabricated 3-D shadow mask is aligned with and inserted into the trench using a flip-chip bonder (Finetech Fineplacer Lambda) in step (3). The shadow mask is placed on the bonder stage while the device wafer is positioned on the bonder arm. The wafer is aligned with the shadow mask, and brought into contact with the mask using a force of 3 N. This force was found to allow complete insertion during successful alignment, but not to cause device or mask damage even in the case of misalignment and insertion failure. Tape-based adhesive is temporarily applied after mask insertion to maintain the contact between the mask and the device wafer, and is removed once the metal deposition is completed. The alignment accuracy of the bonder is 0.5 μm and the registration margins between the shadow mask and the device features are designed to be 10 μm, well within the aligner tolerances. To guarantee a well-defined metal pattern, the height of the spokes on the shadow masks must match with that of the trench within a maximum error of 70 μm, which is achievable since the depth of Bosch etching can be rather accurately controlled.

With the shadow mask inserted, a thick layer of Ti/Cu (1 μm) is then sputtered into the trench, and the subsequent physical removal of the shadow mask results in this layer being patterned both on the vertical sidewall and at the bottom surface, as shown in step (4). To electrically connect the seed layer patterned in individual trenches for subsequent electroplating, a second thin metal deposition (3000 Å) is conducted with silicon donut structures masking the trench area, as shown in step (5). These silicon donut structures are simple 3-D silicon shadow masks that can

be designed to be either individual drop-in masks or an integrated mask wafer with connecting frame between donut structures. In step (6), photoresist is then spray-coated to protect the wafer surface and electroplating is performed to obtain the copper conductors in the trench, from sidewalls to the bottom surface. After photoresist stripping and seed layer removal in step (7), pre-molded solid epoxy donuts are dropped into the silicon trench and melted at a temperature of 130 °C to fill the trench and prepare a planarized surface for top conductor fabrication. After evaporation of a seed layer (Ti/Cu) and photoresist patterning in step (8), electroplating follows to form the top radial conductors. The fabrication process concludes by stripping the photoresist and etching away the seed layer in step (9).

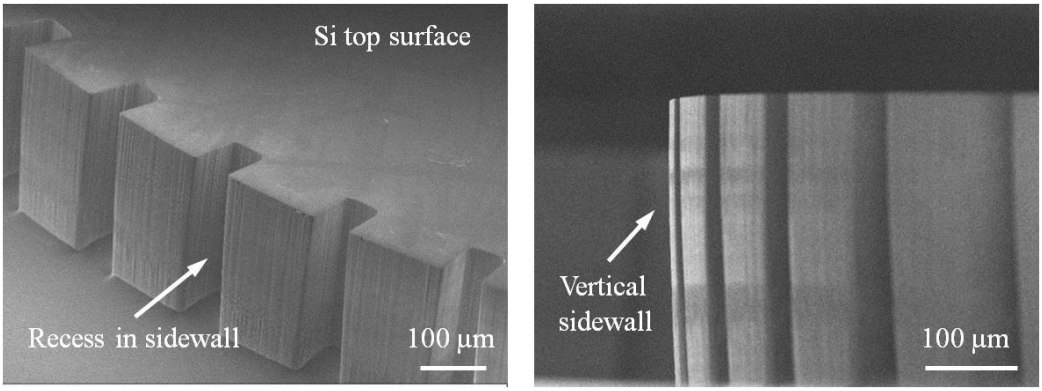


Figure 29: Etched silicon trench with vertical sidewalls in step (2).

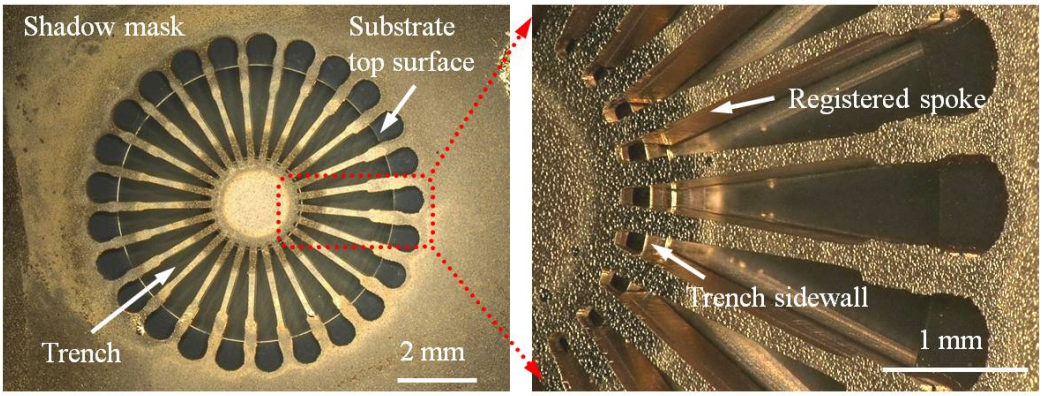


Figure 30: Registered 3-D silicon shadow mask into the device wafer in step (3).

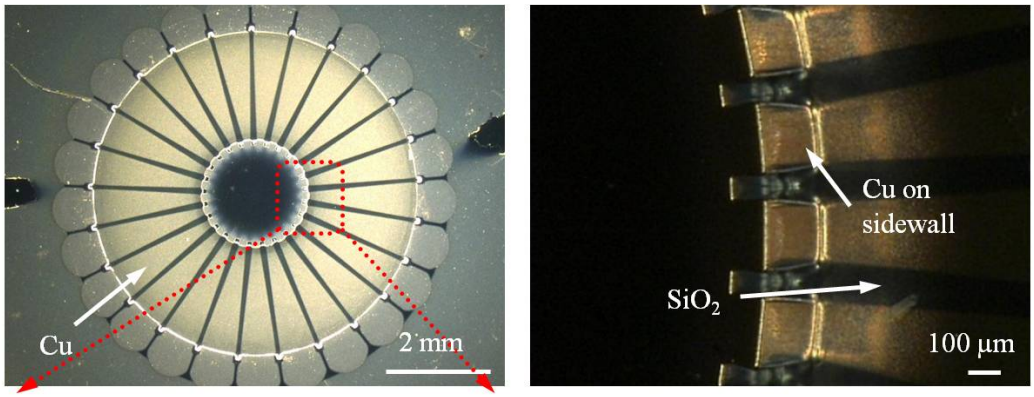


Figure 31: Patterned seed layer on 3-D recessed surfaces of the trench in step (4).

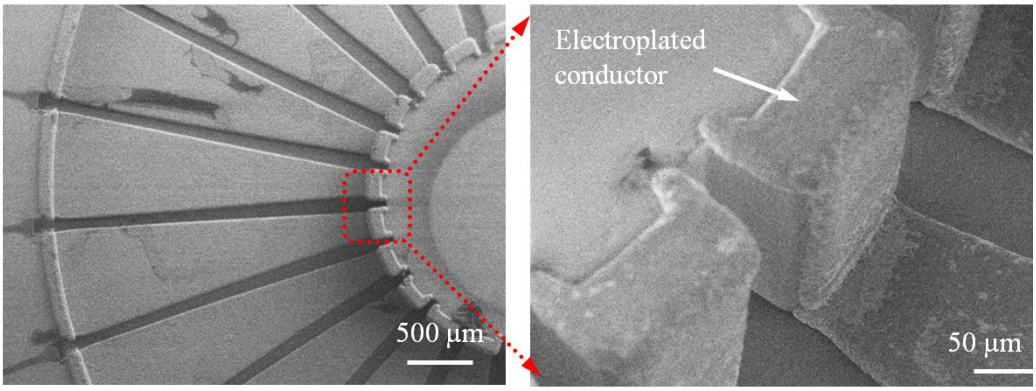


Figure 32: Electroplated vertical and radial conductors in the trench in step (5).

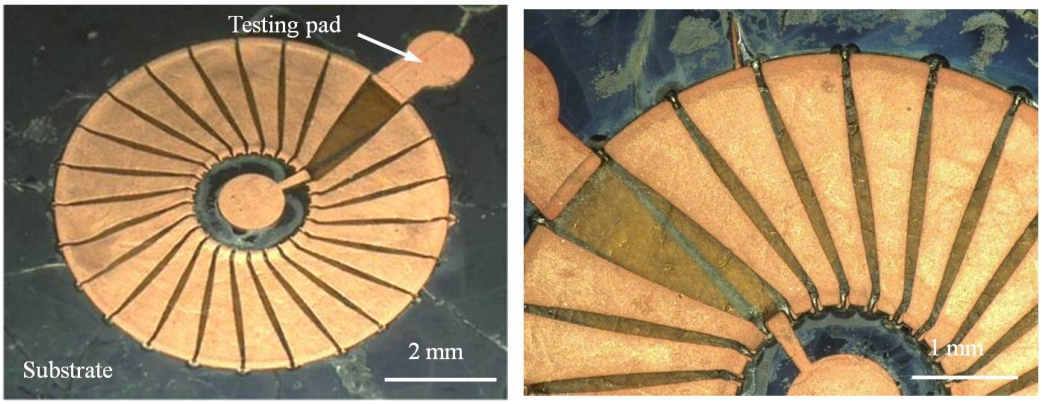


Figure 33: The fabricated inductor embedded in silicon substrate using the 3-D shadow mask-based approach.

Since the vertical copper conductors sit directly on the trench sidewalls in the shadow mask-based embedding design, no complex dry-film technology is needed for fabrication of the top radial conductors as used in the lithography-based approach. In addition, the uncrosslinked epoxy in the trench can be removed easily if required [55], resulting in a real air-core inductor if the epoxy core is not desired. Photomicrographs of the partially-completed devices in selected steps are shown in Figure 29, 30, 31, 32 and the fabricated inductors are shown in Figure 33 with two circular pads of 500 μm in diameter designed for probing and electrical testing. Well-patterned radial conductors with a constant gap of 100 μm at the bottom surface of the silicon trench can be seen clearly through the transparent epoxy. The gap between the top radial conductors gradually widens from the inner and outer edge of the trench to the middle to facilitate timely and uniform etching of the seed layer after electroplating.

3.3 Interconnect Integration

In order to electrically connect the embedded toroidal inductors to circuitry on the wafer front surface, through-wafer interconnects have to be implemented. Due to the power requirements of the DC-DC converters for driving LEDs, these interconnects have to handle current in the order of amperes. The interconnect technique proposed here is compatible with both of the silicon-embedding approaches presented above, and the details for integrating interconnects into the original inductor fabrication processes are shown in Figure 34.

The steps from the original inductor processes are labeled with the same numbers as before and the added steps for fabricating the through-wafer interconnects are labeled in alphabetical order. After silicon trenches are etched into the wafer back side in step (2), through-silicon vias and countersunk trenches for embedding the interconnects on the front side of the wafer can be etched using a patterned photoresist mask and an oxide mask respectively, as shown in steps (a)-(c). Then after forming

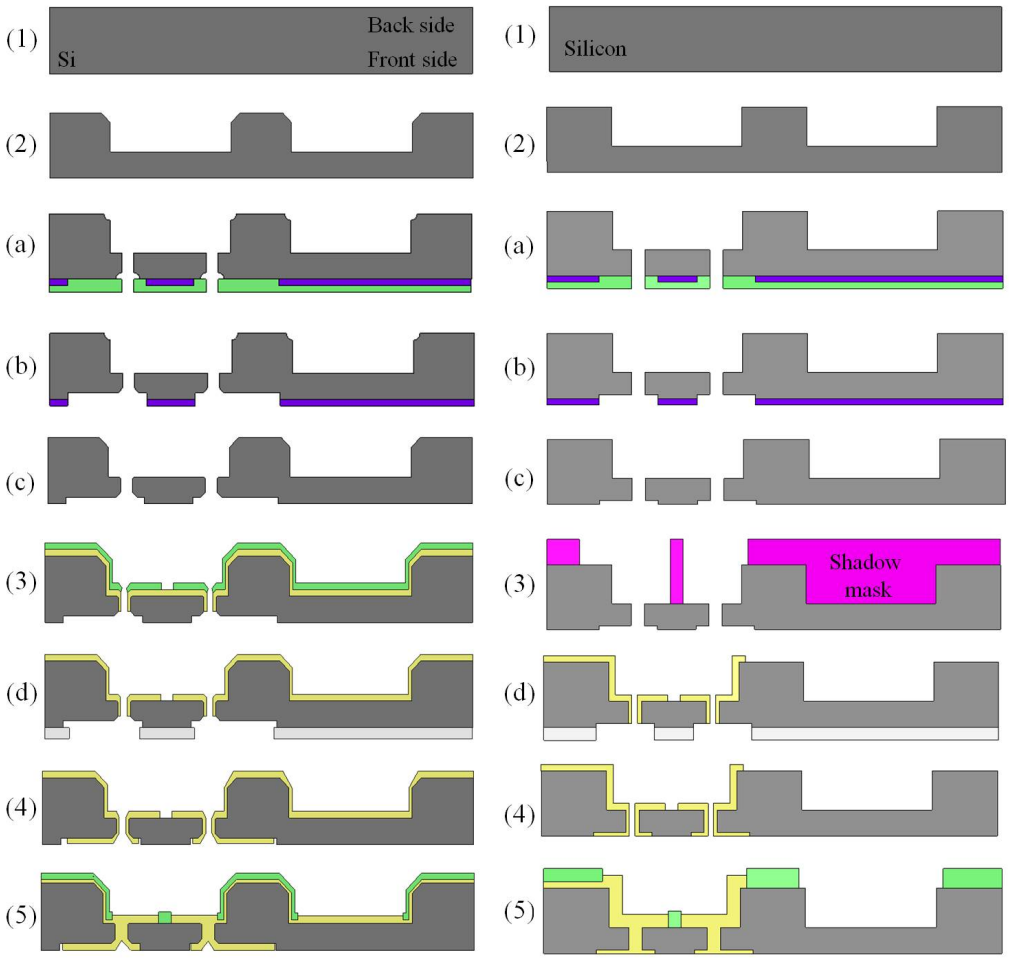


Figure 34: Process integration of through-wafer interconnects with (a) lithography-based approach and (b) shadow mask-based approach.

the patterned seed layer in the trench as before in step (3), metallization of the interconnect trenches is completed through sputtering and lift-off of the dry-film photoresist as shown in step (d)-(4). When electroplating is conducted to form the copper conductors in the silicon trench, the through-wafer interconnects and testing pads are also formed simultaneously, as shown in step (5). The remaining steps for fabricating the inductors are the same as presented before and will not be repeated here.

Results of the fabricated interconnects in selected steps are shown in Figure 35, 36, 37, 38 and the completed inductors with integrated through-wafer interconnects

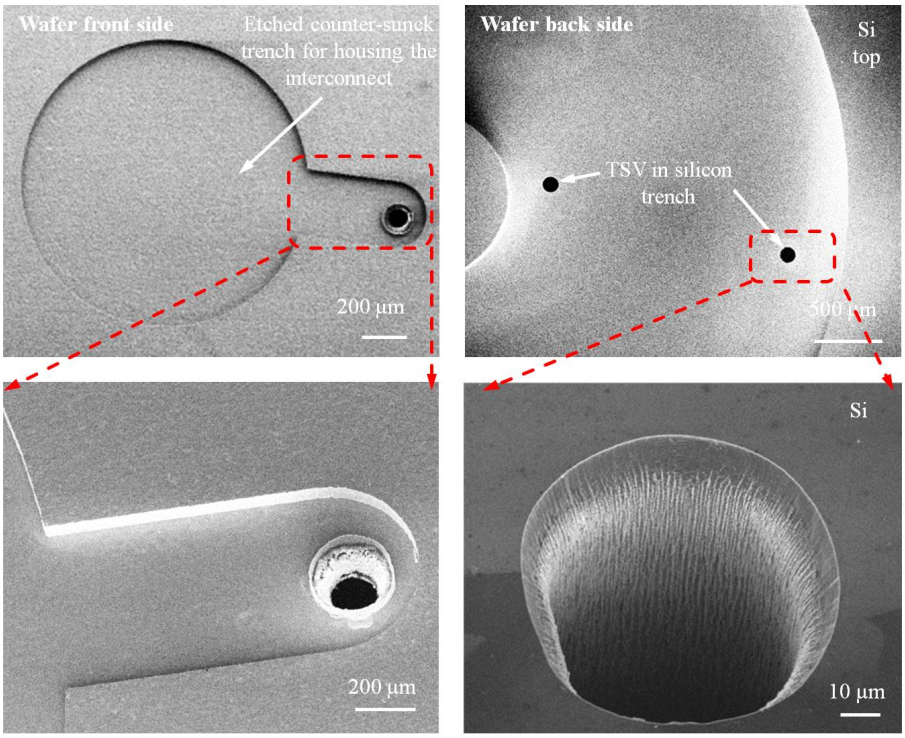


Figure 35: Etched silicon trench with through-silicon vias in step (c).

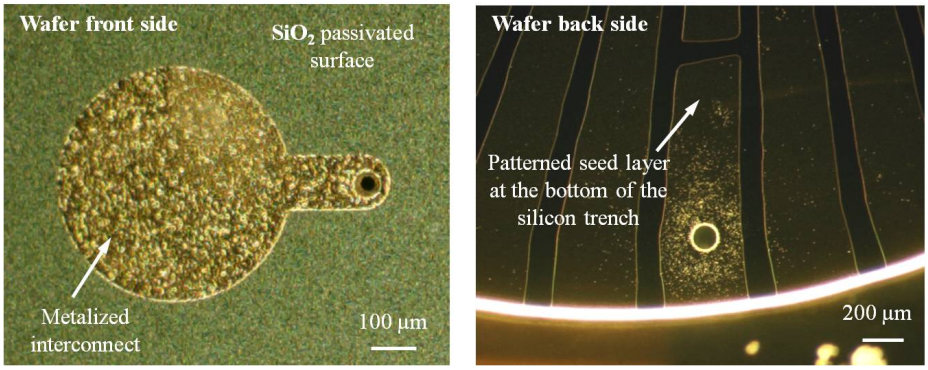


Figure 36: Metalized through-silicon vias and patterned seed layer for conductors in the silicon trench in step (4).

are shown in Figure 39.

3.4 Magnetic Core Integration

Air-core magnetics offer the advantages of avoiding magnetic core losses as well as avoiding the need for a fabrication process incorporating special materials [30], [56],

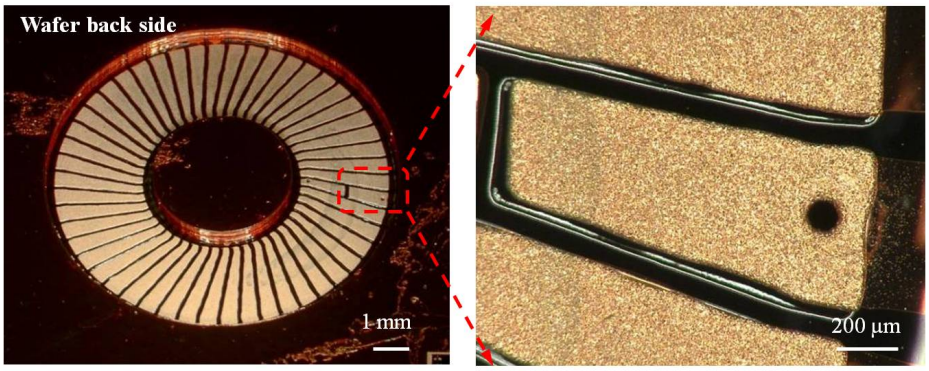


Figure 37: Electroplated conductors in the silicon trench with electroplated through-wafer interconnects in step (5).

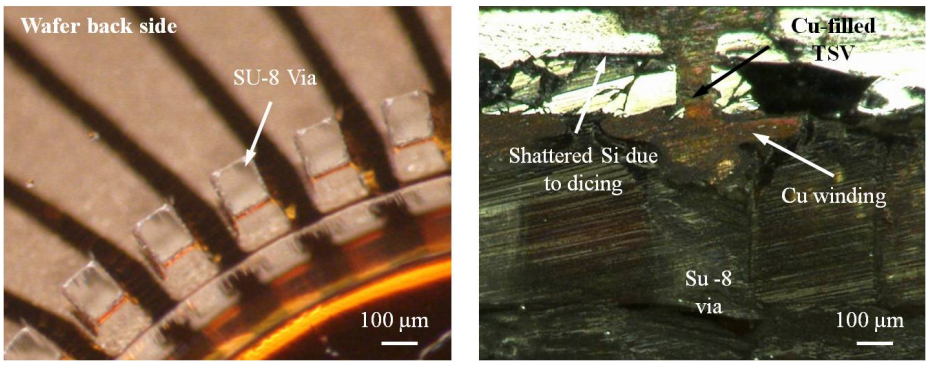


Figure 38: Partially-completed inductors with through-wafer interconnects after SU-8 patterning.

[57], and are suitable for converter circuits operating at very high frequencies since they usually provide limited inductance values. With the addition of the magnetic material, magnetic-core inductors possess increased inductance and quality factor. Magnetic materials usually make it possible to reduce the footprint/height of the inductor needed to achieve high efficiency in power converter.

For high-frequency DC-DC power converters that switch at frequencies of 10 MHz to 100 MHz [21], [58], the required inductance from the integrated inductor varies depending on circuit topologies and power/voltage levels; however, in general, they fall into the range of hundreds of nanohenries. With microfabricated air-core inductors, the realization of hundreds of nanohenries of inductance within a limited

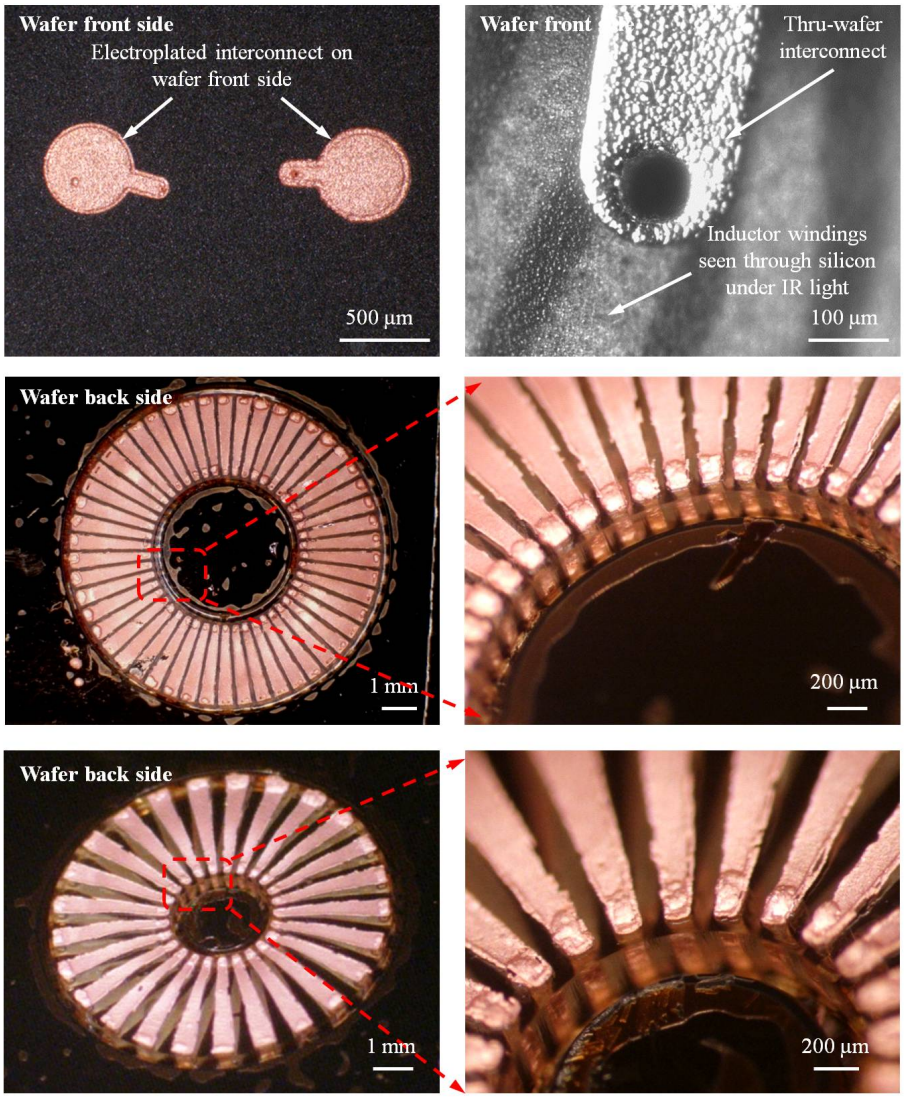


Figure 39: Images of the fabricated inductors with through-wafer high-current interconnects.

volume/footprint is often infeasible due to microfabrication constraints. Even when feasible, such inductance values are usually achieved at the expense of the DC resistance of the inductor and its current handling capability. To address this problem, soft magnetic material can be employed as a magnetic core to boost the inductance of the embedded inductor and enhance its performance. Monolithic fabrication processes for integrating inductors with various magnetic materials have been reported [14], [37], [40].

Based on the developed silicon-embedding techniques, core integration can be achieved by dropping in appropriately-shaped materials at the midpoint of the winding fabrication process [59]. Since the magnetic cores are prepared separately from the winding fabrication process, the drop-in approach allows the use of various well-developed magnetic materials.

Figure 40 illustrates the detailed core integration process based on the shadow-mask approach. A partially-completed inductor with lower and vertical windings fabricated within a silicon trench is first prepared as shown in step (a) using the 3-D shadow-mask approach. In parallel, a toroidal magnetic core with appropriate

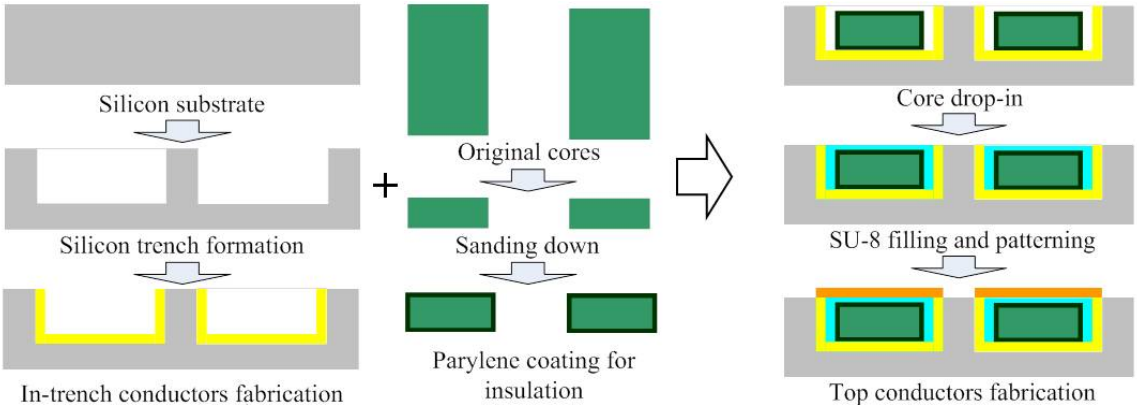
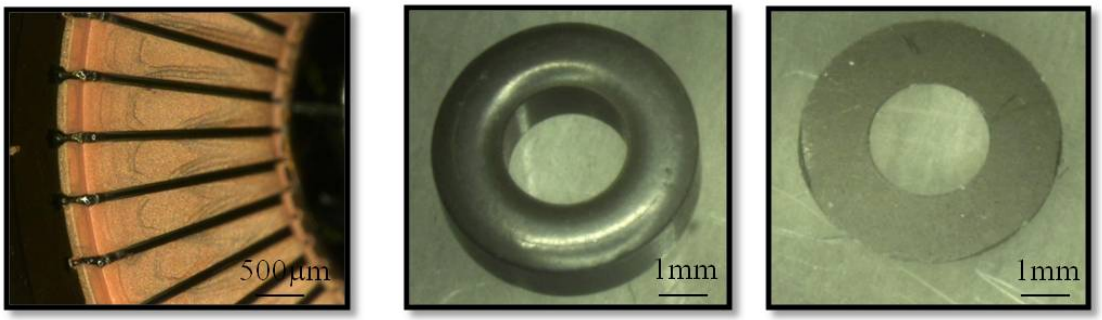


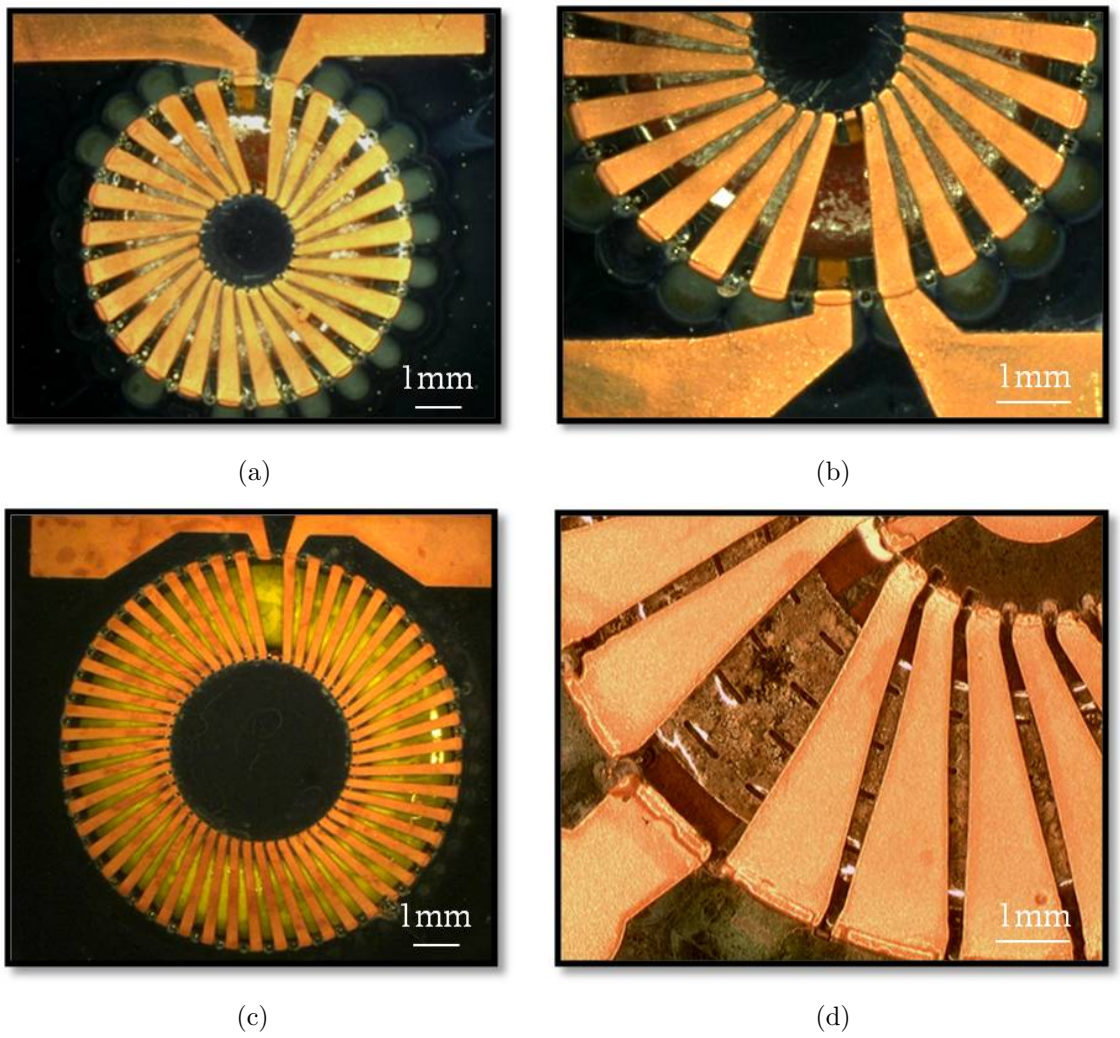
Figure 40: Fabrication process of silicon-embedded inductors with dropped-in magnetic cores.



(a) (b)

Figure 41: A partially-completed inductor with bottom and vertical windings (a) and an iron powder core from Micrometals (b): before and after lapping.

magnetic properties and thickness is identified in step (b). If the magnetic core is thicker than the desired inductor height (for example, commercial iron powder/ferrite cores typically have a thickness in millimeter scale), it should be thinned prior to integration, which can be achieved by lapping for iron powder and ferrite cores. A photomicrograph of a partially-completed inductor with bottom and vertical windings and an iron powder core before and after lapping is shown in Figure 41. The core thickness before and after lapping is 1.78 mm and 200 - 250 μm respectively. The inner diameter of this core is 2.24 mm and the outer diameter is 5.08 mm. Upon completion



(a) (b)

(c) (d)

Figure 42: Fabricated silicon-embedded toroidal inductors with integrated iron powder cores (a)-(c) and a metallic CoNiFe core (d).

of the lapping, a 5-μm-thick parylene layer can be deposited onto the core to ensure electrical insulation between the inductor windings and the core during integration. This insulation layer may not be necessary if the selected magnetic core has high resistivity, as in the cases of some iron powder cores and NiZn ferrites. However, it may need to be thickened when low-resistivity metallic cores are employed. After the magnetic core is insulated, it is dropped into the partially-completed inductor as shown in step (c). Solid SU-8 epoxy pieces are then melted at 130 $^{\circ}C$ to fill in the trench; lapping of SU-8 can be conducted to achieve planarization if necessary and cross-linking of the SU-8 follows to secure the core. Fabrication of the top conductors, as introduced in the shadow-mask approach before, then completes the device.

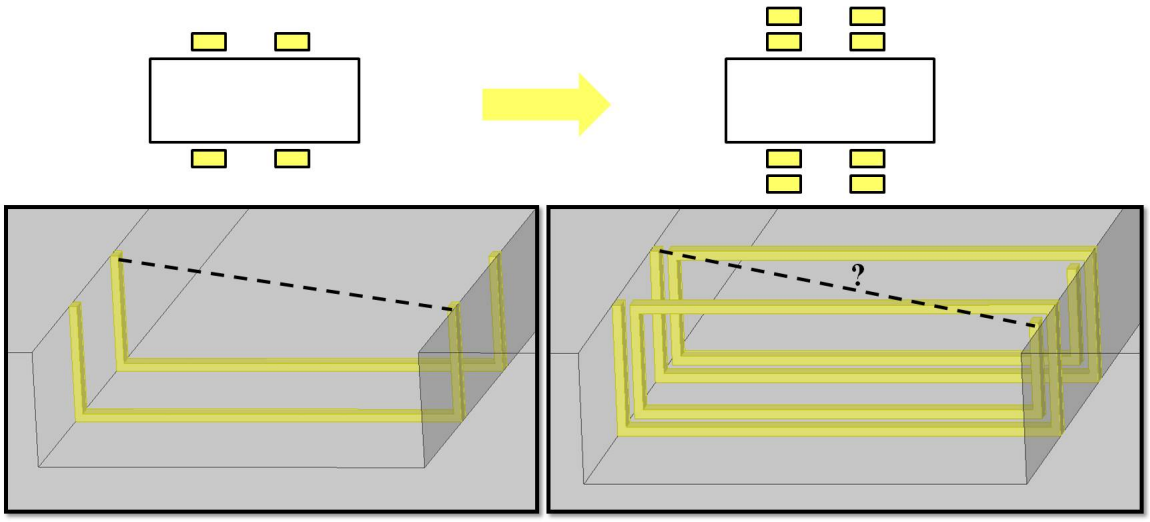
Photomicrographs of fabricated inductors with various integrated cores are shown in Figure 42. The inductor height is in the range of 250-300 μm and the thickness of the core is approximately 200-250 μm. The copper thickness in the device is approximately 30 μm.

3.5 Double-Layer Winding Structure

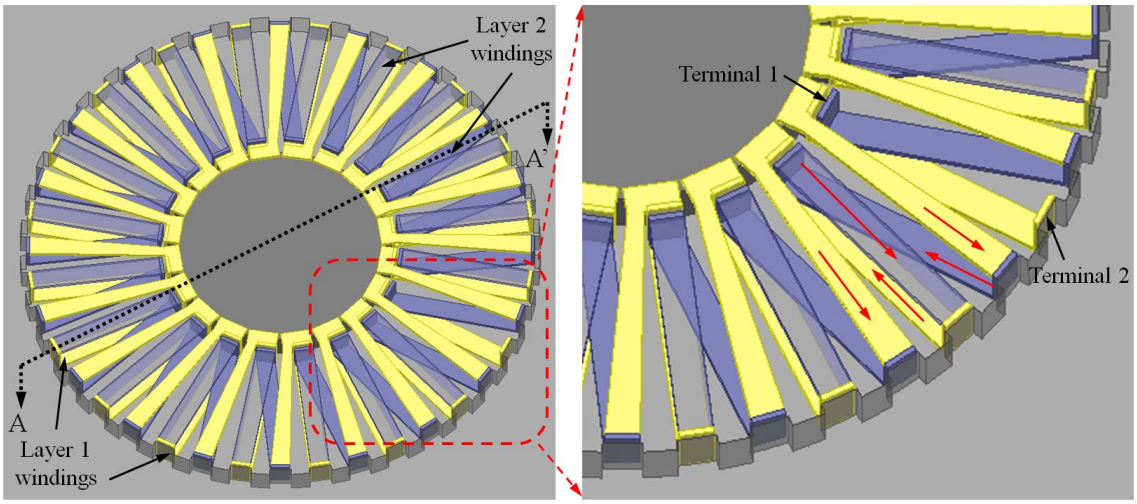
So far, the micromachined inductor structures that have been presented have only single-layer windings. Although discrete inductor components often have multiple layers of windings wound around a magnetic/non-magnetic core to boost the inductance, it is hard to implement multi-layer windings in microfabrication due to the complex processing difficulties. While the technology we developed for embedding 3-D devices into deep silicon trenches enables on-chip integration of toroidal inductors with a tall profile, the patterning resolution on top of 3-D recessed surfaces is limited compared to patterning on planar surfaces. Since the inner diameter is significantly smaller than the outer diameter in a toroidal design, the feature sizes along the inner diameter are significantly smaller than anywhere else, and therefore constrain the maximal number of turns that can be put into the inductor. Together with the fact

that the center area in the toroidal inductor does not contribute to the inductance of the device, unlike solenoid and planar inductors, toroidal designs often exhibit a lower inductance density, which could result in a non-sufficient inductance for our targeted applications.

To enhance the inductance density and overcome the patterning resolution constraints on the inner diameter of the toroidal inductors, embedded inductors with



(a)



(b)

Figure 43: Embedded toroidal inductor with double-layer winding design, (a) the concept of implementing double-layer windings, (b) detailed geometry design.

double-layer winding designs are proposed based on the 3-D shadow mask approach, as shown in Figure 43. The concept behind the double-layer winding design is shown in Figure 43 (a), with a comparison to the previous single-layer design. Basically, in a double-layer winding design, the conductors will complete two loops instead of one loop in the trench before going to the next turn. Therefore, the number of the windings in the embedded inductor will be doubled without changing the footprint and height of the inductor. However, since one of the vertical conductors will be buried under a top conductor after completing two loops in the same turn, it is difficult to connect the buried vertical conductor to the non-buried vertical conductor in the adjacent double-layer turns, as shown in the right drawing of Figure 43 (a). To solve this problem, the two-layer inner vertical conductors are designed to be overlapped with each other while the outer vertical conductors are not overlapped, as shown in Figure 43 (b). Therefore, no outer vertical conductors will be buried under the top conductor connecting other outer vertical conductors, which can be seen from the conduction path as illustrated by the red arrows in the magnified view of Figure 43 (b), and single-layer top conductors can be designed to complete the conduction loop and save fabrication efforts. The blue color in the figure denotes the windings on the inner layer of the conduction loop and the yellow color denotes the windings on the outer layer of the conduction loop in the trench. The second-layer vertical and bottom conductors are fabricated directly on top of the first-layer conductors with an insulation layer between them based on our previously-developed shadow mask approach. Since the two-layer inner vertical conductors overlap with each other completely, it reduces the constraints of the patterning resolution on the inner diameter as well.

Using the pre-manufactured 3-D shadow masks, the detailed process for fabricating the embedded toroidal inductors with double-layer windings are shown in Figure 44 with both 2-D drawings of the cross-sectional cut through the line AA' shown in

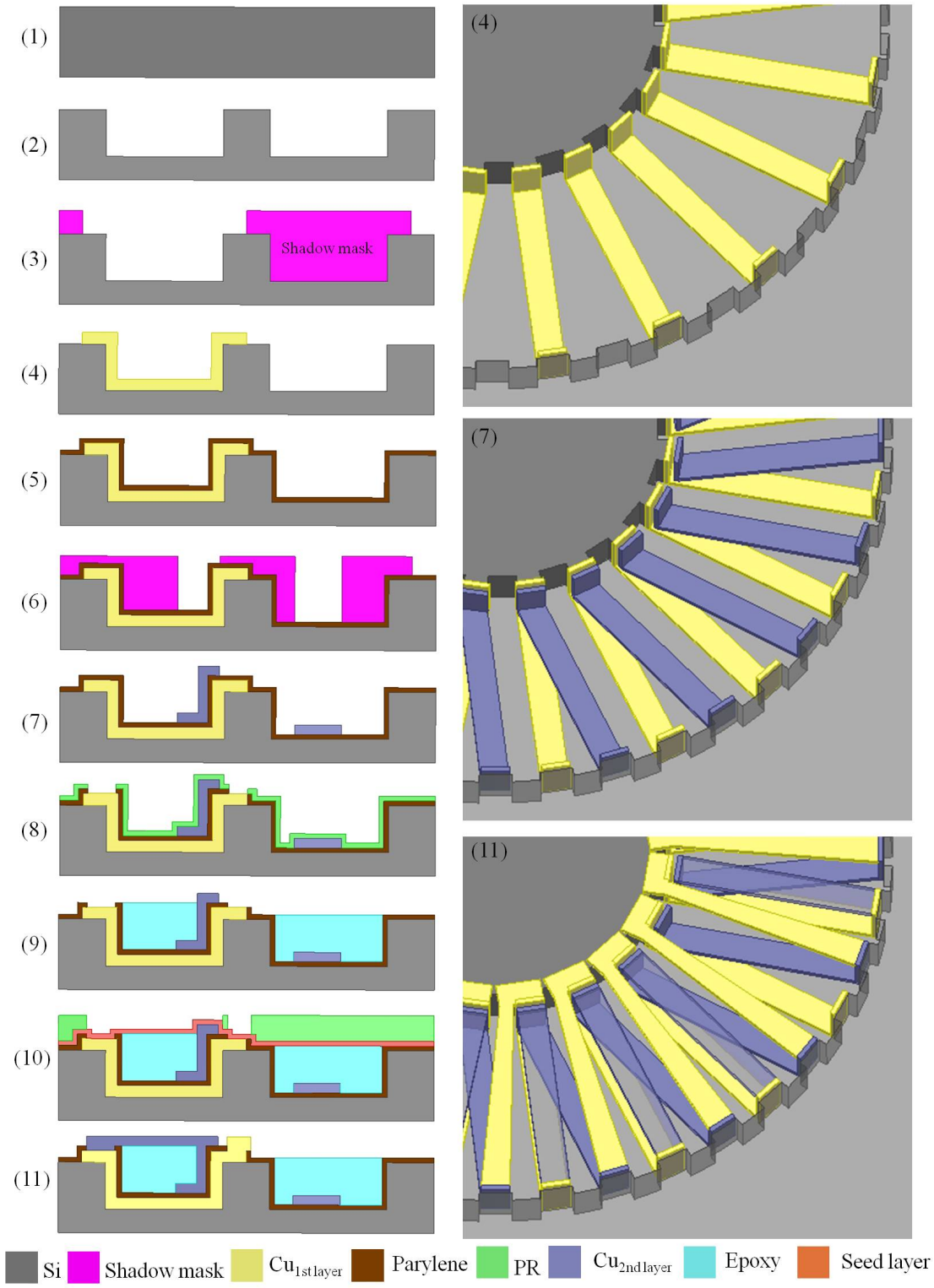
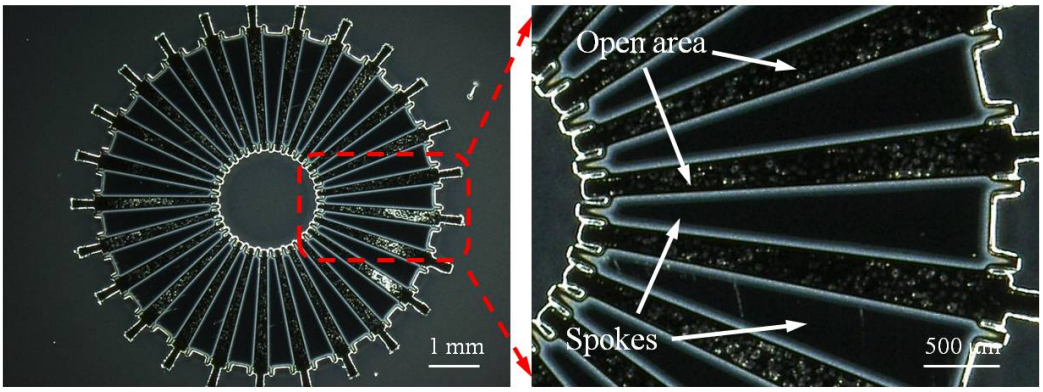
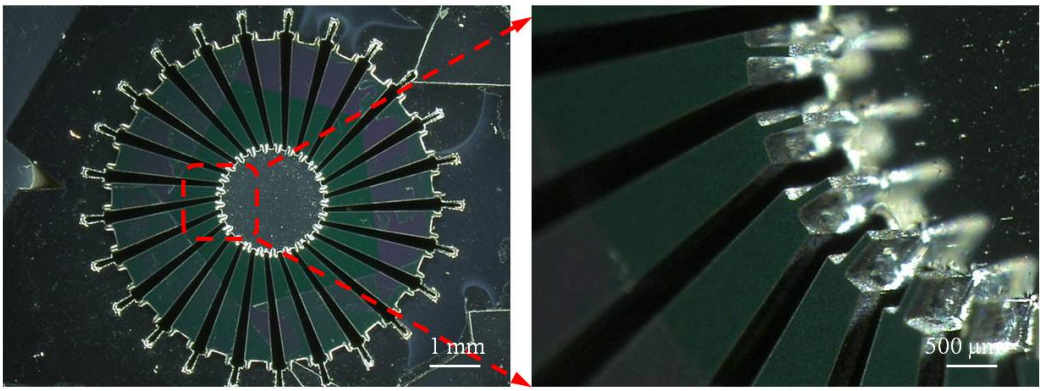


Figure 44: Fabrication process of the embedded inductor with double-layer windings: 2-D cross-sectional drawings and 3-D drawings in selected steps.

Figure 43 (b) and 3-D drawings shown for selected steps. Starting with a standard 4-inch silicon wafer in step (1), silicon trenches are first etched into the substrate through Bosch process in step (2). After passivation of the wafer, a 1.5-μm-thick seed layer (Ti/Cu) is sputtered into the trench using the 3-D shadow mask designed for the first-layer windings and electroplating follows to form the first-layer bottom and vertical windings, as shown in step (3) and (4). Then after photoresist removal and seed layer etching, a 10-μm-thick parylene layer is deposited onto the wafer in step (5), protecting the completed first-layer windings during the formation of the



(a)



(b)

Figure 45: Fabricated 3-D shadow masks for defining the first-layer windings (a) and the second-layer windings (b).

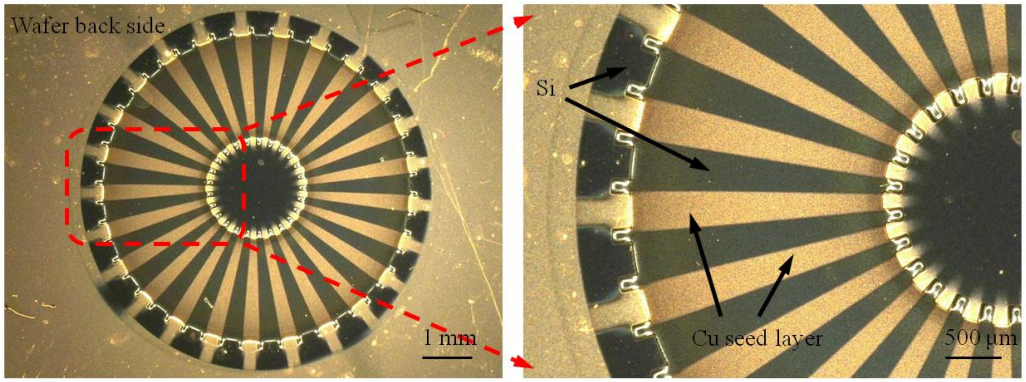


Figure 46: Patterned seed layer for the first layer of copper windings.

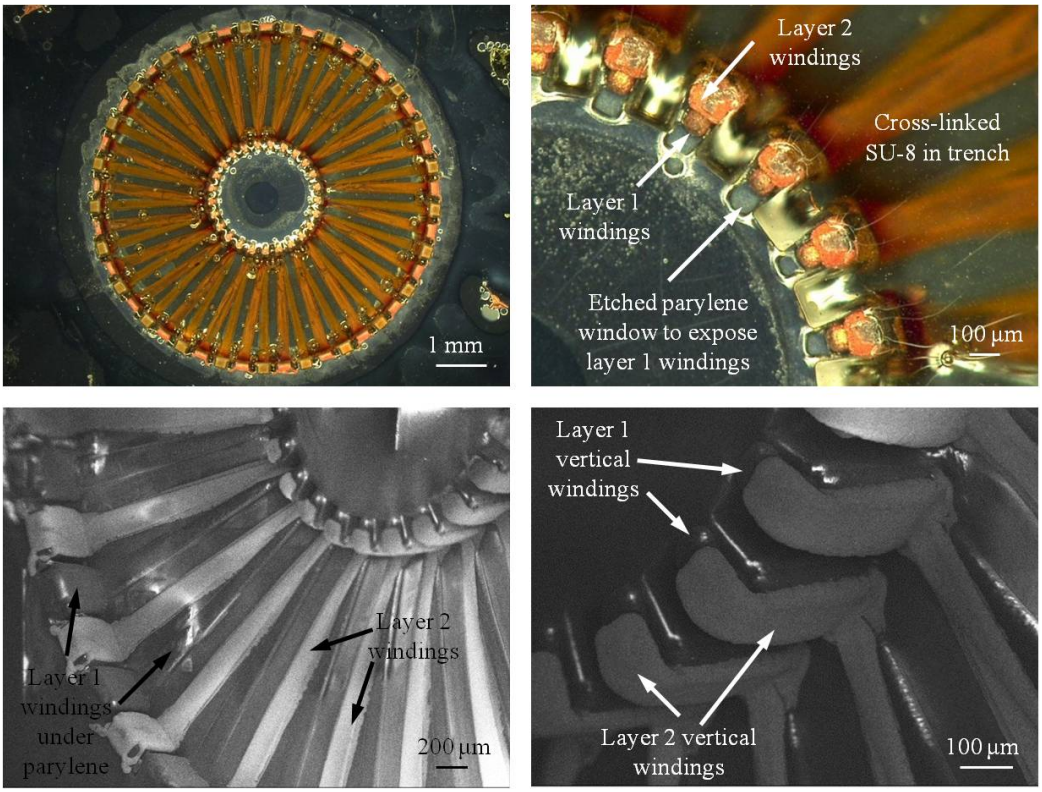


Figure 47: Electroplated two-layer bottom and vertical windings.

second-layer windings. In step (6), the 3-D shadow mask designed for the second-layer windings can be used to define the sputtered seed layer (Ti/Cu, 2.5 μm thick) on the parylene surface and electroplating can be conducted to form the second-layer

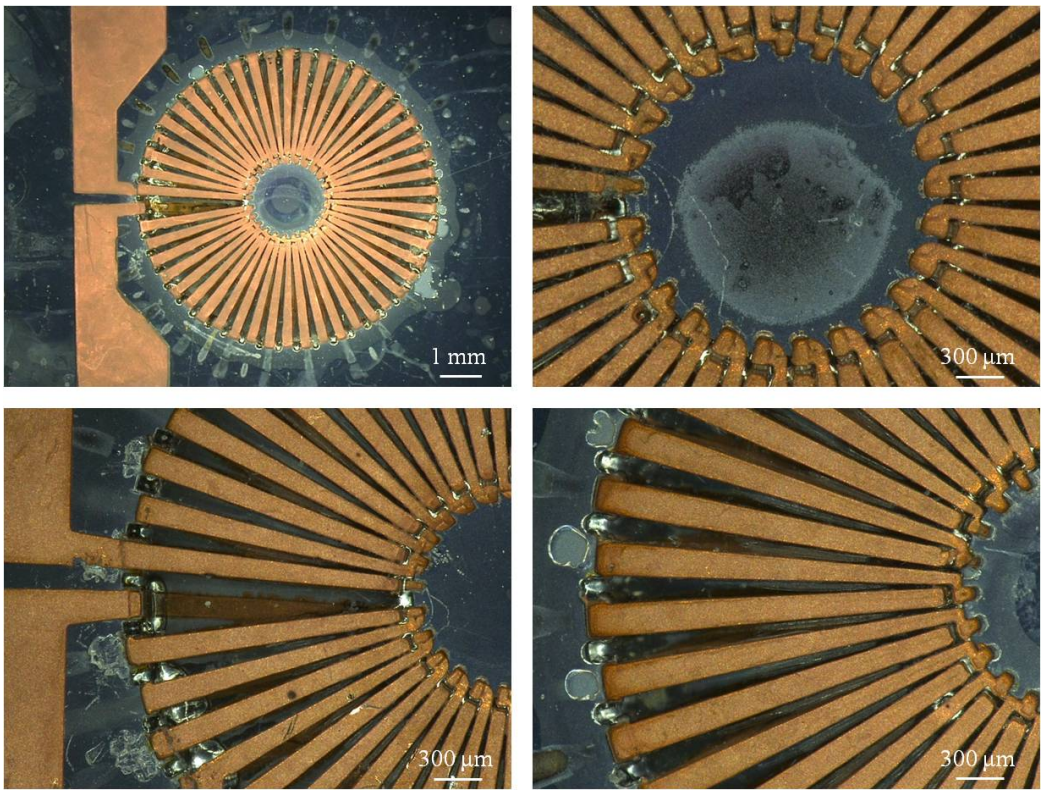


Figure 48: The fabricated silicon-embedded toridal inductors with double-layer windings.

inductor windings, as shown in step (7). After patterning a spray-coated layer of photoresist as the mask, parylene is etched using oxygen plasma to expose some parts of the first-layer windings in order to make connection to the top conductors, as shown in step (8). Solid SU-8 epoxy is then melted and patterned in the trench after stripping the photoresist mask in step (9). With evaporated seed layer and spray-coated photoresist as the mold in step (10), the top conductors for connecting the double-layer vertical and bottom windings are electroplated, completing the conductor path. With photoresist removal and seed layer etching, the device is completed as shown in step (11).

Images of the pre-manufactured 3-D shadow masks for the first-layer windings and second-layer windings are shown in Figure 45. Photomicrographs of the partially-completed inductors in selected steps are shown in Figure 46, 47, and images of the

completed inductors are shown in Figure 48. The inner diameter of the inductor is 2 mm and the outer diameter is 6 mm. The inductor height is approximately 300 μm. The copper thickness in the device is approximately 20 μm.

3.6 Summary

In this chapter, MEMS technology for enabling embedding of 3-D functional structures into the silicon volume on the backside of the wafer is introduced. Two different approaches for fabricating the 3-D structures in deep silicon trenches are developed, the lithography-based approach and the 3-D shadow mask-based approach, with each having its own advantages and limitations.

By using well-established conventional techniques, the lithography-based approach enables batch fabrication of the devices and offers great design and fabrication flexibility. In this approach, there are no techniques that are specific to the inductor device itself, such as spray-coating techniques, proximity lithography, thick SU-8 patterning, and dry-film lithography. Therefore, the same set of techniques can be potentially applied to fabricate other 3-D devices with device-oriented adjustments. Further, devices with different embedding depths can also be realized from batch to batch without changing the masks.

However, due to the processing of thick SU-8 epoxy that is needed in forming the mold for housing the vertical copper conductors, the lithography-based approach is time-consuming. Tens-of-hour electroplating is also required to fill such a thick SU-8 mold to form the vertical conductors. Besides, special care needs to be taken during patterning steps on top of the cross-linked SU-8 structures because SU-8 structures tend to delaminate due to its thermal expansion mismatch with silicon when there is elevated temperatures, such as during baking steps and metal deposition steps. The thickness of the thin silicon layer that remains on top of the embedded device has to be sufficient to withstand the possible stress that builds up in the silicon due to the

shrinkage/expansion of the cross-linked SU-8 epoxy and not too fragile to hamper the wafer handling. The uniformity of the silicon dry etching process (around 10 μm variation in our case) also needs to be taken into consideration when determining the thickness since it affects the thickness uniformity and mechanical strength of the thin silicon layer. Depending on the mechanical strength of the integrated chip required, constraints on the thickness of the remaining silicon layer has to be understood prior to device design and fabrication.

In the shadow-mask approach, based on the structure of the toroidal inductors, special features are designed on the 3-D shadow mask to ensure that the vertical conductors in the toroidal inductor can be formed simultaneously with the bottom radial conductors during one copper electroplating step, eliminating the multiple lithography steps, thick SU-8 patterning process, and bottom-up electroplating of the SU-8 vias and therefore reducing the overall process time significantly compared to the lithography-based approach. The fact that the shadow-mask process is less complex also leads to a higher yield of devices in fabrication than the lithography-based approach. Although fabrication of the shadow mask does take time, the shadow mask can be reused to produce multiple device wafers. Besides, since there is no gap between the embedded device and the sidewall of the silicon trench, and the top surface of the embedded device is fabricated coplanar with the substrate in the shadow-mask approach, the integrity and mechanical strength of the integrated chip is better maintained. The direct contact of conductors with silicon (with a silicon dioxide layer in between) also results in a better heat dissipation of the device during in-circuit operation since silicon is a better heat sink compared to epoxy. In addition, when considering the core integration and development of double-layer winding structures, the shadow-mask approach is also more compatible compared to the lithography-based approach.

While the shadow mask approach offers great benefit in many aspects, care should

be taken to ensure high processing quality in forming the shadow masks. For example, any dirt or residues that are not removed from the wafer surface prior to DRIE etching will act as masks in the dry-etching step and generate defects that prevent the shadow mask from being in good contact with the device wafer. In addition, the height of the embedded inductor and the number of the masks that can be put into one shadow-mask wafer is also limited by the fragility of the mask. Since the thickness of the silicon framework connecting individual shadow masks is determined by the wafer thickness and the height of the spokes, with a given wafer thickness, the taller the spokes (which is desirable for taller devices and higher inductance), the thinner the silicon framework. With this thin silicon framework, the shadow-mask wafer can also become increasingly fragile with an increasing number of devices incorporated. To address this problem, a reinforcing outer frame can be designed to help strengthen the shadow-mask wafer, which is maintained at the original substrate thickness, as shown in Figure 49. For demonstration here, six shadow masks are fabricated in a 100-mm-diameter wafer with a reinforcing outer frame that has the original substrate thickness. The robustness of the outer frame greatly facilitates the mask handling,

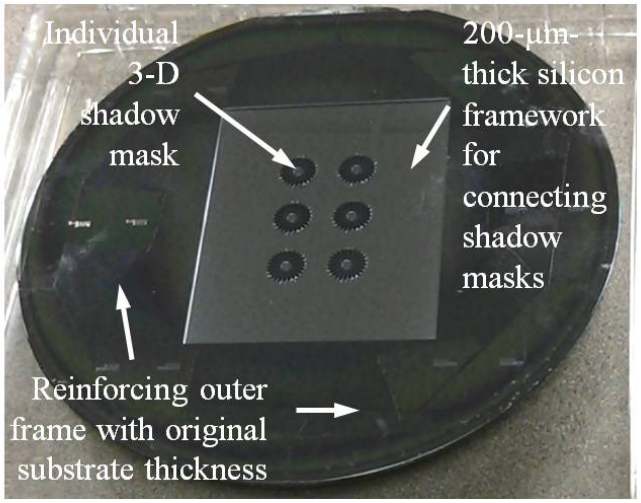


Figure 49: A 3-D shadow-mask wafer with a reinforcing outer frame.

insertion, and removal during the inductor fabrication process. Fabricated shadow-mask wafers have been reused over thirty times without failure. Further, it should be emphasized that this process is batch-fabrication compatible, as six devices are fabricated simultaneously with a single 100-mm-diameter mask insertion. Denser packing, smaller devices, and larger/thicker mask wafers could enable more masks to be incorporated into the wafer, and therefore result in a greater batch-fabrication throughput.

CHAPTER IV

EMBEDDED INDUCTOR DESIGN AND MODELING

After the silicon-embedding technologies are developed, the next step in enabling embedded inductors for integrated power converter applications is to understand how to design the inductors that meet the circuit performance requirements.

4.1 Circuit Topology

Since inductor characteristics depend strongly on the circuit topology and performance, details of our targeted converter circuit, where the inductor needs to operate, are first introduced here.

A merged-two-stage circuit topology suitable for efficient LED drivers operating from a wide-range dc input voltage in the high-frequency (HF) regime (3-30 MHz) is developed by our collaborators in the ARPA-E program [15], as shown in Figure 50. This two-stage approach is based on a soft-charged switched-capacitor pre-regulator/transformation stage and a high-frequency magnetic regulator stage.

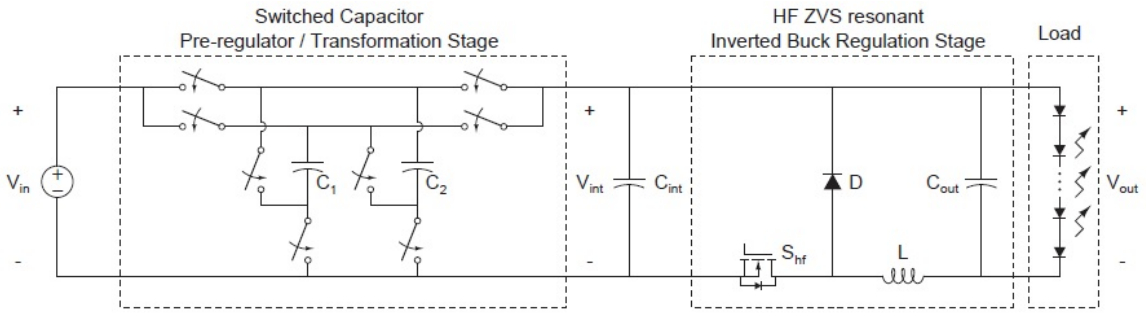


Figure 50: A merged two-stage conversion architecture having a switched capacitor first stage that provides voltage pre-regulation and transformation, and a high-frequency magnetic stage that provides fine regulation of the output [15].

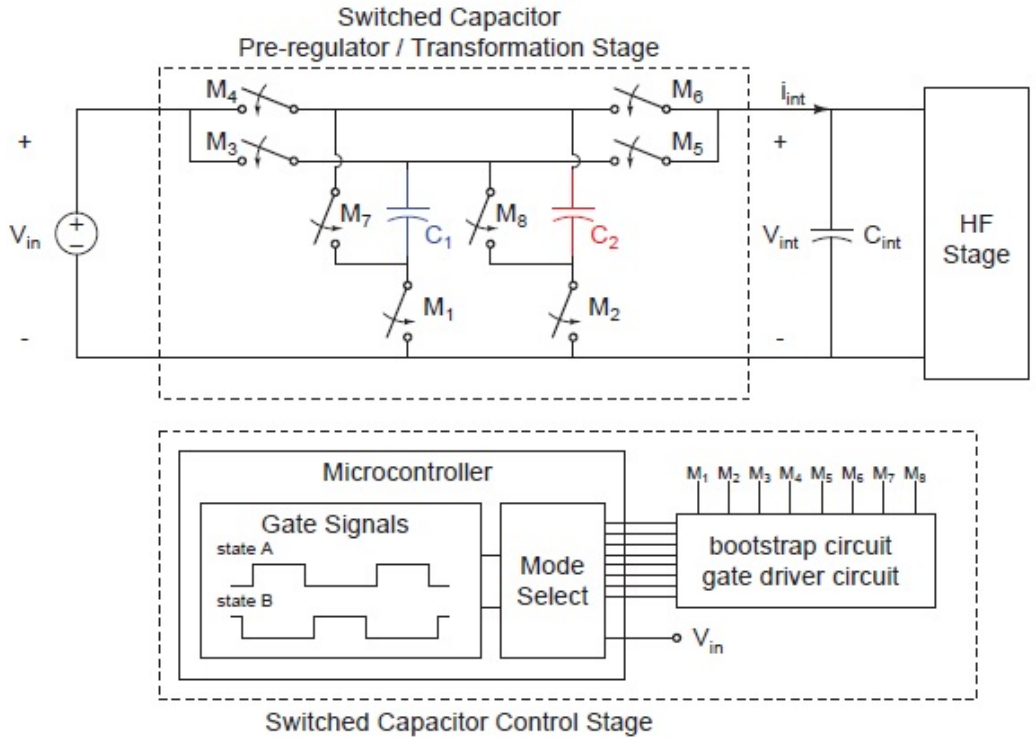


Figure 51: Schematic of the switched capacitor pre-regulator/transformation stage of the merged two-stage converter [15].

The first stage, that is, a variable-topology switched-capacitor (SC) circuit, operates at moderate switching frequencies, such as tens to hundreds of kHz. The details of the circuit with the controller design is shown in Figure 51. It is realized with energy transfer capacitors (C1-C2) and power transistors (M1-M8), which are controlled to turn on and off by a micro-controller at a fixed frequency with 50% duty ratio. The SC circuit can achieve high power density and efficiency. However, the SC converter alone cannot efficiently provide the fine voltage regulation capability needed in this application. This stage serves both to reduce the voltage range over which the second stage needs to operate, and to reduce the maximum voltage level for which the second stage must be designed.

The second stage is a magnetic-based stage that provides both additional voltage transformation and fine voltage regulation, and is operated at high frequency such

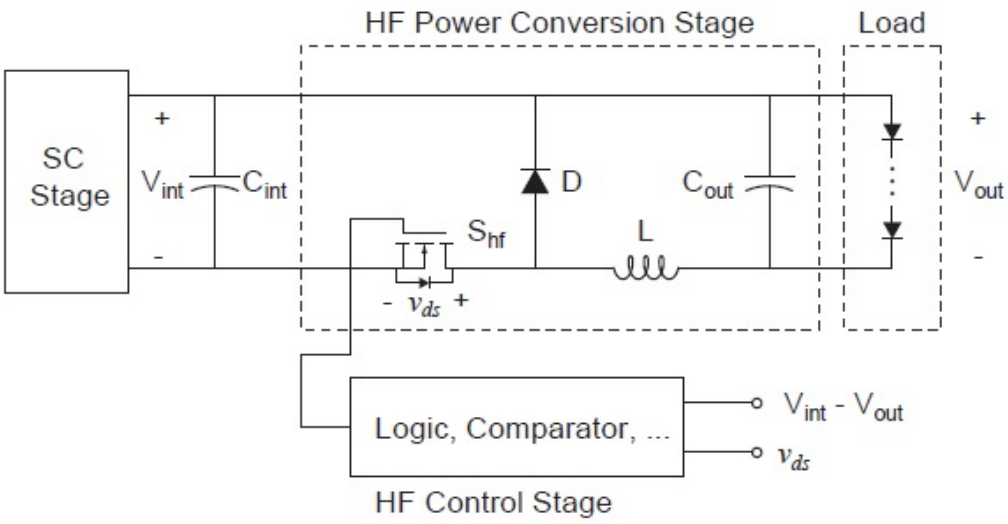


Figure 52: Schematic of the second magnetic-based regulation stage operating at high frequency [15].

as 3-30 MHz in order to minimize the magnetic component size. The topology of the second stage is selected such that it requires relatively small inductor values and inherently absorbs parasitic capacitance as part of circuit operation, as shown in Figure 52. Many converters operating from high voltages at low powers (tens of watts) suffer from large-valued inductors. A benefit of this topology is that it operates with high inductor current ripple, yielding a relatively small value of inductance and small magnetic energy storage. Moreover, as the system architecture enables a relatively low value of V_{int}, the needed value of inductance is further reduced. Lastly, the soft-switched nature of the circuit topology enables relatively high switching frequency to be achieved with acceptable loss, further reducing the required inductance value.

In summary, soft charging of the switched capacitor circuit, zero voltage switching of the high-frequency regulator circuit, and time-based indirect current control are used to maintain high efficiency, high frequency and power density, and high power factor for our targeted applications.

4.2 Inductor Requirements

Inductor characteristics are mainly described by two parameters, inductance and quality factor (or loss). Inductance defines the energy storage capability of an inductor and quality factor describes how lossy an inductor is. There are also other design parameters such as saturation current (if there are magnetic cores), breakdown voltage and heat dissipation capability that should be examined about the inductor once the inductance and quality factor requirements are met.

In general, with switch-mode buck converters, the minimum required inductance by the converter circuit is a function of its operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current, as shown in equation (1):

$$L = \frac{V_{out}(V_{in} - V_{out})}{V_{in} \cdot f \cdot I_{p-p}}, \tag{1}$$

where V_{in} is the input supply voltage, V_{out} is the converter output voltage, f is the switching frequency, and I_{p-p} is the peak-to-peak current.

From the equation, higher peak-to-peak inductor current allows for a lower inductance value. A lower inductance minimizes size and cost and improves large-signal and transient response of the circuit. However, the circuit conversion efficiency is reduced due to high peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor.

A higher inductance increases circuit efficiency by reducing the ripple current; however, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions.

Since the required inductor characteristics depend strongly on the circuit topology and performance, and the circuit performance depends strongly on the inductor characteristics as well, co-optimization of the circuit and inductor is needed [60], as

shown in Figure 53. Given performance objectives such as conversion efficiency, input voltage, output voltage, output power, etc., circuit simulation is performed to determine the requirements on inductor performance at the desired frequency such as inductance and maximum allowed loss. Then the inductor design process is conducted to find a feasible design for meeting the requirements. The circuit simulation can then be performed again based on the specific inductor design to predict the corresponding circuit performance. If a feasible design could not be found based on the specified inductor requirements, for example, due to fabrication limits, different switching frequencies can be selected and circuit simulation can be conducted again to find a new set of requirements. This process can be iterated until feasible designs are found.

Based on our targeted circuit topology as discussed in the section above, a numerical circuit simulator is implemented in computationally efficient functions in the MATLAB programming language [16]. The circuit simulation begins by specifying

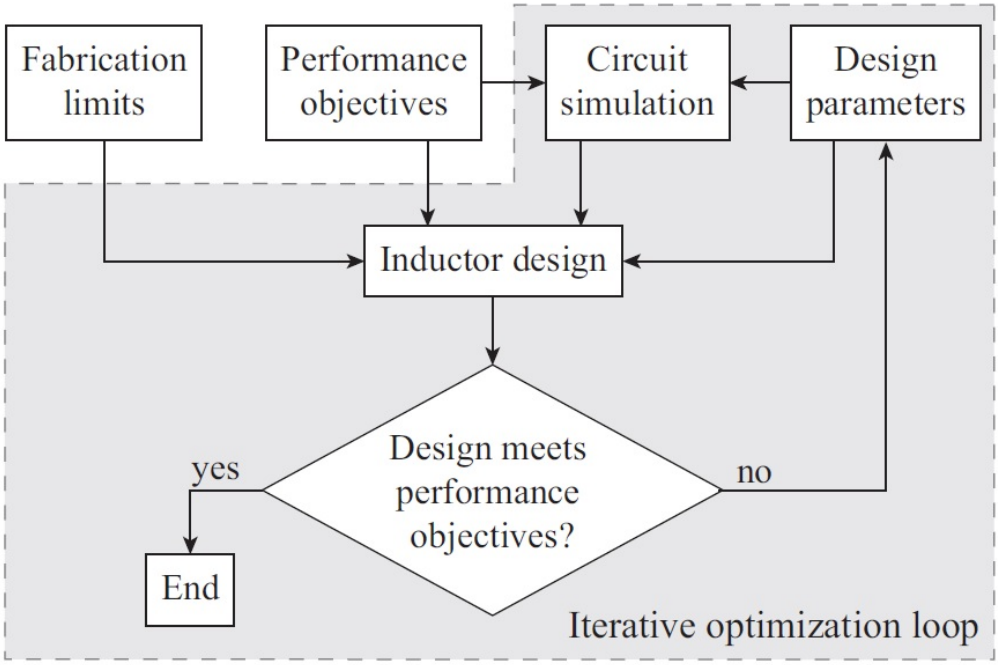


Figure 53: Co-optimization approach for circuit and inductor design [16].

the converter objectives of input and output voltage, and output power. These are the fixed inputs to the circuit simulation. There are also input variables that characterize the converter FET and diode, including the FET output capacitance, the FET on-state resistance, a resistance in series with the FET capacitance, the diode forward voltage drop, the diode junction capacitance, and the resistance in series with the diode capacitance. These input variables have initial fixed values. However, the simulation is capable of optimally scaling the FET channel width to minimize semiconductor losses.

Once the operating frequency and inductor capacitance is chosen, the circuit simulation determines the inductance required to process the specified power at the specified voltages given the specified operating frequency and transistor characteristics. The simulation also produces current and voltage waveforms within the converter from which the inductor losses can be calculated, the FET and diode losses used for calculating the total circuit efficiency, and the optimized scaling factor of the FET channel width.

4.3 Inductor Design Methodology

Upon determination of the required inductance and allowed inductor losses by the converter circuit, a methodology is needed to guide the inductor design and optimization process in order to find an embedded inductor with the proper geometry that meets the performance standards.

In 2012, Han et al., reported a design procedure for integrating low-permeability ferrite cores into printed circuit board (PCB) coils for high-frequency power applications [61]. Extrapolating this procedure directly to the microfabrication regime, however, poses challenges due to the presence of different constraints.

Embedding toroidal inductors into silicon imposes volumetric and microfabrication constraints that put additional limitations on inductor design parameters and

complicate the trade-offs to be made in designing the embedded inductors:

1. The maximum achievable copper thickness for the embedded inductor windings is often limited by fabrication technology and device geometry, which leads to a non-negligible winding resistance that is less frequently a concern in PCB inductors and wire-wound inductors.

2. On-chip integration and silicon embedding of the toroidal inductors puts volumetric constraints on the device footprint and height. The inductor should neither occupy an area larger than the chip, nor possess a height exceeding the thickness of a silicon substrate.

3. A limited footprint and patterning resolution implies that only a limited number of turns can be fabricated, imposing a limit on the maximum inductance that can be achieved. In addition, a tradeoff between the inductance and resistance needs to be considered since squeezing more turns into the inductor results in increased resistive loss that may affect the device performance.

These constraints dictate an unusual design and optimization methodology for embedded inductors compared to wire-wound inductors and PCB inductors. As a result of these constraints, the design problem we are trying to solve becomes:

"For a given footprint and a targeted inductance value, can we design a silicon-embedded inductor (with air core or magnetic core) that satisfies fabrication constraints and achieves the required quality factor at the desired frequency?"

4.3.1 Air-Core Embedded Inductors

To tackle the problem, air-core inductors are first considered.

The inductance and quality factor of an embedded toroidal inductor can be calculated from the following equations:

$$L_{air} = \frac{\mu_0 N^2 h}{2\pi} \ln \frac{d_o}{d_i}, \tag{2}$$

$$Q_{air} = \frac{\omega L_{air}}{R_{Cu} + R_{sub}}, \tag{3}$$

where L_{air} stands for the inductance of the embedded air-core inductor, N is the number of turns in the inductor, h is the inductor height (or the depth of embedding into the substrate), d_o, d_i are the outer and inner diameter of the toroidal inductor respectively, Q_{air} is the quality factor of the air-core inductor, ω is the angular frequency with $\omega = 2\pi f$ where f is the switching frequency, R_{Cu} denotes the losses coming from the copper windings in the embedded inductor and R_{sub} denotes the losses induced by the silicon substrate.

Given the targeted inductance value,the required number of turns in the inductor can be calculated from equation (2) after determining the desired inductor geometric parameters under fabrication constraints. The achievable quality factor can then be estimated using equation (3) providing that the losses in the inductor are understood for the calculated number of turns at the frequency of interest. This process can be iterated to explore the design space comprised of geometric parameters until an optimal or satisfactory design is obtained.

Since the inductor footprint is given, d_o is a fixed value in equation (2). h should be chosen to be the maximum depth that could be etched into the substrate, which also becomes a fixed value once the substrate is selected because the larger the value of h, the better the device performance. Consequently, what's left in equation(2) that could be varied is d_i. However, the selection of d_i is often constrained by patterning resolution and fabrication technology.

If the quality factor calculated from equation (3) is not sufficient based on the selected design parameters, the losses in the embedded inductors need to be understood in order to determine the right optimization strategy in improving the design results. Depending on the significance of the different losses in the embedded toroidal inductor, there are two different optimization strategies.

- Regime A: If the substrate-induced loss R_{sub} is comparable to the copper loss

R_{Cu} or dominates, substrate loss should be suppressed first to see if the design performance is satisfactory instead of focusing on geometry optimization of the inductor itself.

- Regime B: If the substrate-induced loss R_{sub} is negligible compared to the copper loss R_{Cu} or has been suppressed to be, optimization of the inductor geometry is now the focus to reduce the winding losses, such as selecting a different inner diameter, increasing copper thickness, increasing winding width, and reducing resistive losses, etc.

Although the inductance of toroidal inductors can be estimated with good accuracy using well-developed formulae in literature, the losses in the embedded inductor are more difficult to predict due to the complex electromagnetic phenomena that could arise at high frequencies, which makes the critical process of estimating the device quality factor difficult.

4.3.2 Loss Mechanisms

To estimate the winding loss and substrate-induced loss, different loss mechanisms existing in the embedded inductors need to be understood first. Depending on the origins of the losses in silicon-embedded inductors, they can be divided into two categories: magnetically-driven losses and electrically-driven losses. Magnetically-driven losses are related to the magnetic field generated in the inductor, often with leakage components penetrating into the substrate as well, which lead to eddy current loss in the copper windings as well as in the substrate if the substrate is conductive. Electrically-driven losses are caused by the electric field that exists in both the inductor and the substrate due to voltage drops; such losses include ohmic loss in the windings and parasitic coupling loss that arise from the voltage difference present at the winding-to-winding and winding-to-substrate proximity [62], [63]. Although the

loss estimation problem can be addressed by means of numerical modeling, quasi-analytical approaches can be useful to gain design insight [14]. To make the problem more tractable for quasi-analytic modeling, the relative significance of these losses is first analyzed.

To estimate the eddy current loss in the inductor windings, various analytical models have been developed in the literature [64]–[66]. For example, a model to estimate the eddy current loss in toroidal inductor windings with low-permeability cores has been studied [65] based on Dowell's model that estimates copper loss due to the skin effect [64]. However, when using these analytical models, care should be taken since these models are usually not universally applicable. Finite element modeling (FEM) can also be used to predict the inductor loss accurately, although it takes a significant amount of computational effort.

The eddy current loss induced in the silicon substrate at our frequency of interest (3-30 MHz) is negligible [67] because toroidal design offers a good confinement of the magnetic flux in a closed path and the leakage flux from the bottom and vertical windings into the substrate is limited.

Among electrically-driven losses, ohmic loss in the inductor windings is represented by the DC resistance of the inductor, which can be calculated based on the winding geometry and usually does not contribute to a significant part of the inductor losses at high frequencies. However, parasitic coupling losses can have a dramatic impact on the inductor performance.

Parasitic coupling loss varies with frequency, inductor geometry and the properties of the substrate. Lumped element models have been developed to take into account the parasitic capacitances and resistances from the silicon substrate for surface-micromachined RF planar inductors [68]. However, there is a lack of models for describing the embedded toroidal inductors.

In embedded inductors, the major parasitic capacitance stems from the proximity

of the copper conductors to the silicon substrate because typically these conductors have large area and are insulated from the silicon substrate by a thin insulation layer (e.g., PECVD-deposited SiO_2). The existence of parasitic resistance is due to the finite conductivity of the silicon substrate. These parasitics form a network through which the electrical signal can be coupled, and therefore generate substrate loss that could exceed the copper loss in some cases. To minimize the losses associated with substrate parasitics, removing the silicon completely or partially under the embedded planar inductor was demonstrated to be effective [11], [13]; however, this approach is not suitable for our approach where power converter circuitry is to be manufactured on the silicon above the embedded toroidal inductor. Adding a metal shielding layer between the inductor and the substrate can reduce the parasitic coupling effect [69]. However, it also leads to a lowered device inductance, and additional losses can be introduced in the shielding layer.

With these complicated loss mechanisms existing in the embedded inductors at high frequencies, the ability to understand the significance of different losses, model the silicon-embedded inductors, and predict their performances is required for the inductor design and optimization process.

4.3.3 Loss Modeling

A distributed equivalent circuit model is proposed to explore the loss characteristics of the silicon-embedded toroidal inductors at our frequencies of interest. The circuit model provides a simplified way to gain insight into the two major loss components in the embedded inductor: copper loss in the inductor windings and substrate loss due to parasitic coupling.

Since winding losses haven been studied extensively in the literature, various well-developed analytical models can be used to model the copper loss in the toroidal windings [64], [65], [67], [70], [71]. Substrate-induced parasitics are estimated based

on the inductor geometry and the electrical properties of the embedding materials. These parasitics are then used to estimate values for the elements in the distributed circuit model, which is then simulated to obtain the losses attributable to parasitics.

The proposed circuit model takes the geometric design of the inductor and the electrical properties of the embedding and insulating materials as input, and outputs the frequency-dependent inductance, resistance and quality factor of the inductor at an operating frequency of interest. This model also predicts the magnitudes of the losses in the inductor windings and in the substrates separately. In this model, we take the embedded inductor as a turn-by-turn-based distributed set of magnetically-linked turns. Each turn is modeled as a lumped element possessing a single-turn inductance, single-turn resistance and single-turn parasitics that are translated from the geometric and material information of the turn based on a physical model for the turn. An equivalent circuit model of the entire inductor can then be derived as a network of lumped-element parameters. With the estimated values for single-turn lumped-element parameters, the equivalent circuit model is then simulated in Hspice at the targeted frequency, and the complex impedance of the embedded inductor is obtained, from which the inductance and resistance of the inductor can be derived. The details of this modeling procedure are presented as follows.

The proposed physical model for extracting the parasitics of the embedded conductors in the silicon trench is shown in Figure 54(a) [72]. Each single turn in the toroidal inductor includes a bottom conductor, a top conductor and two vertical conductors and is designed to be identical except for the two terminating turns that connect to the testing pads. Since the area of the vertical conductors in contact with the substrate is small compared to the area of the the bottom conductor, parasitics induced by the vertical conductors can be ignored. The top conductor is in far proximity from the silicon substrate, and so does not contribute to substrate parasitics. Therefore, our physical model only considers bottom conductors, and two of

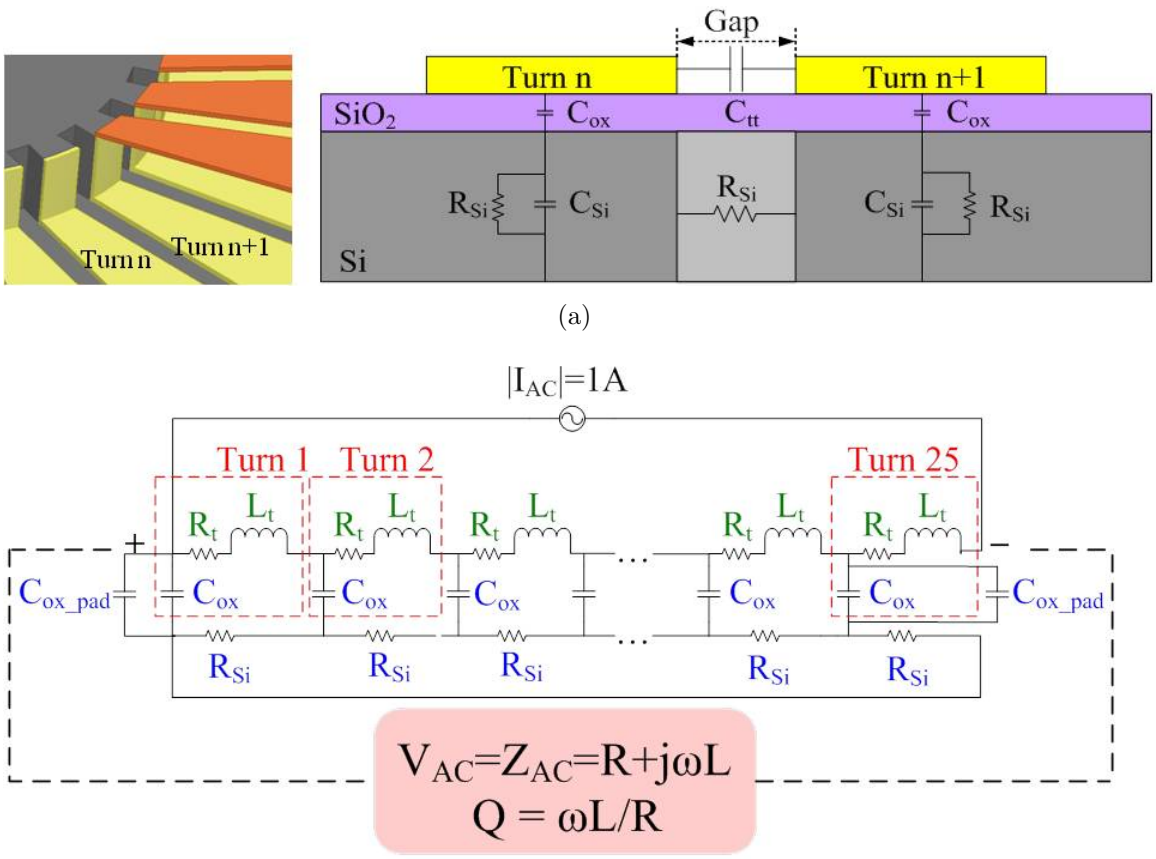


Figure 54: Illustration of (a) a physical model for two adjacent turns and (b) the simplified distributed circuit model for an embedded inductor that has 25 turns as an example.

the adjacent bottom conductors in the trench are shown in the figure as as example.

The parasitic capacitance existing between a single inductor turn and the silicon substrate C_{ox}, can be estimated as:

$$C_{ox} = \frac{\varepsilon_{ox} A_t}{d_{ox}}, \tag{4}$$

where ε_{ox} is the permittivity of the oxide insulation layer, A_t is the conductor area in contact with the substrate and d_{ox} is the thickness of the oxide layer. C_{ox-pad} is the parasitic capacitance between the testing pads and the substrate, estimated using the same formula. The turn-to-turn parasitic capacitance C_{tt} and the oxide-to-substrate

capacitance C_{Si} is small compared to C_{ox} and therefore is ignored in the simplified distributed circuit model, as shown in Figure 54 (b).

Since the substrate thickness is comparable to the width of the conductor, the parasitic resistance R_{Si} can be estimated from the silicon bulk under the adjacent conductors using

$$R_{Si} = \frac{\rho l_{tt}}{A_{Si}}, \tag{5}$$

where ρ is the resistivity of the silicon substrate, l_{tt} is the distance between adjacent conductors and A_{Si} is the cross-sectional area of the silicon bulk.

By taking each turn as a lumped element with a single-turn inductance, single-turn resistance and single-turn parasitics based on the proposed physical model, an equivalent distributed circuit model of the entire inductor can be obtained in Figure 54 (b).

Since the single-turn inductance elements are defined as coupled inductors in H-spice in order to account for the fact that all the inductor turns share the same magnetic flux and therefore have the same induced voltage difference, the single-turn inductance L_t can be obtained from:

$$L_t = L/N^2, \tag{6}$$

where N is the number of turns, and L is the overall inductance of the toroidal inductor, which can be estimated from equation (2).

The single-turn resistance R_t can be obtained from:

$$R_t = \frac{R}{N}, \tag{7}$$

where R can be estimated using Dowell's method.

By supplying the two terminals of the embedded inductor with an AC current source having a unit magnitude, the distributed circuit model is simulated in Hspice over the frequency range of 100 kHz to 100 MHz and the voltage across the inductor,

which equals the complex impedance Z_{AC} of the inductor, is calculated. The equivalent resistance (R) and inductance (L) of the embedded inductor can subsequently be obtained from the real and imaginary part of the complex impedance. The quality factor can then be calculated.

Following this approach, the characteristics of toroidal inductors both with and without silicon embedding are simulated and the results are shown in Figure 55. All the simulated inductors have the same geometrical design, that is, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, a turn number of 25, and a copper thickness of 30 μm.

The non-embedded inductor stands for the inductor design without a lossy substrate, for example, it can be a design on a glass substrate. In such an inductor, there are no substrate parasitics, and consequently no substrate coupling loss. The simulated quality factor of the non-embedded inductor increases monolithically with frequency, while that of the inductor embedded in silicon with a 1.2-μm-thick oxide insulation layer is degraded at frequencies above 10 MHz, illustrating the detrimental impact of substrate parasitics at high frequencies.

Upon verifying the parasitic coupling loss, the possibility of reducing the substrate parasitics to an extent not affecting the inductor performance at frequencies above 10 MHz is examined through modeling. Based on the equivalent circuit model, without changing the inductor winding design itself, there are potentially two ways to reduce the substrate coupling effect: reducing the parasitic capacitance C_{ox} and optimizing the parasitic resistance R_{Si}.

Under practical fabrication consideration, the possibility of increasing the thickness of the insulation layer to reduce the parasitic capacitance is first examined without changing the inductor winding design, substrate resistivity or the insulation material (PECVD-deposited SiO_2). The corresponding simulation results are shown in Figure 56. The inductors possess the same geometry as before: 25 turns, an inner

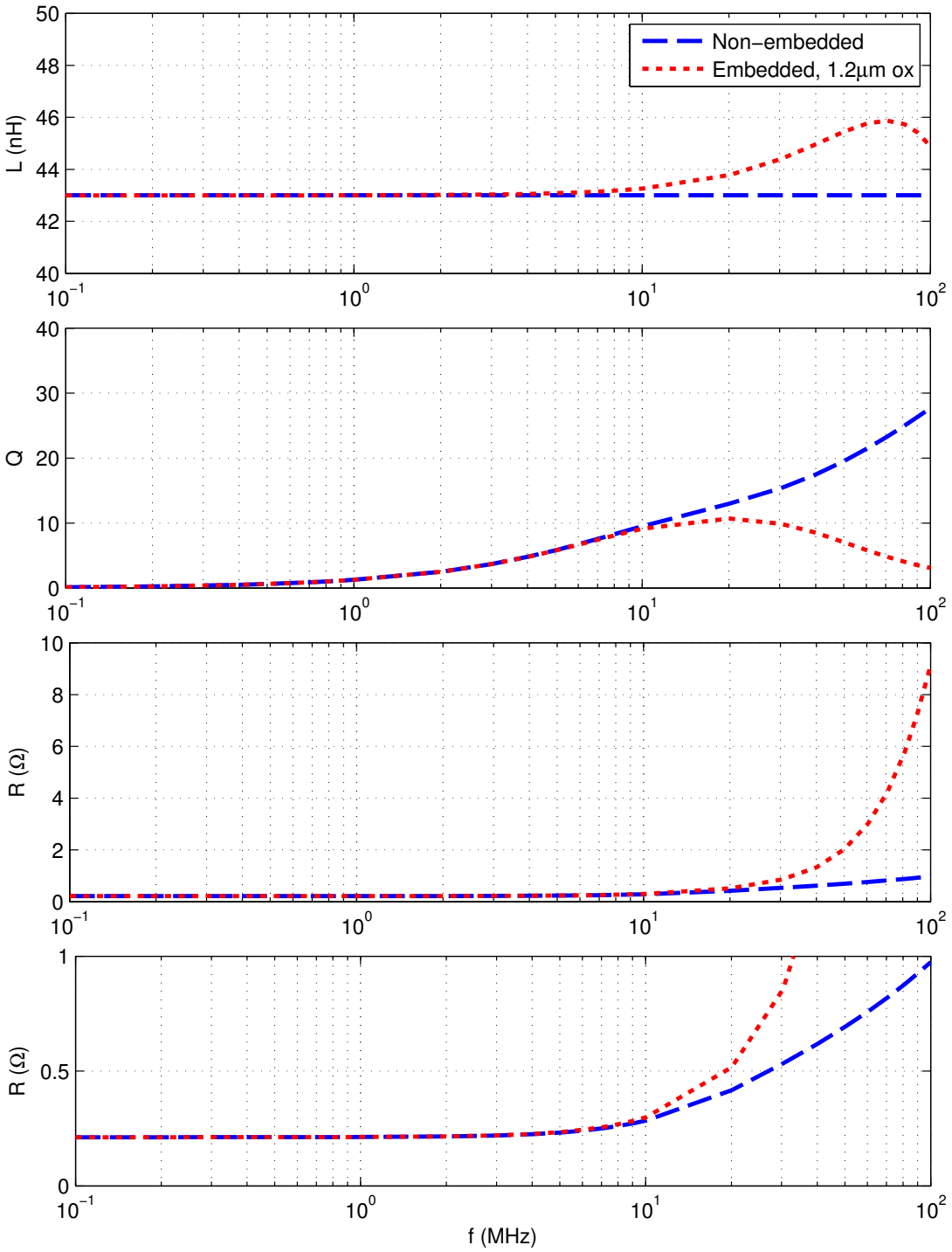


Figure 55: Simulated inductance (L), quality factor (Q) and resistance (R) of the non-embedded and embedded inductor in a standard-resistivity (1-30 $\Omega \cdot cm$) silicon substrate passivated with 1.2-μm-thick SiO_2.

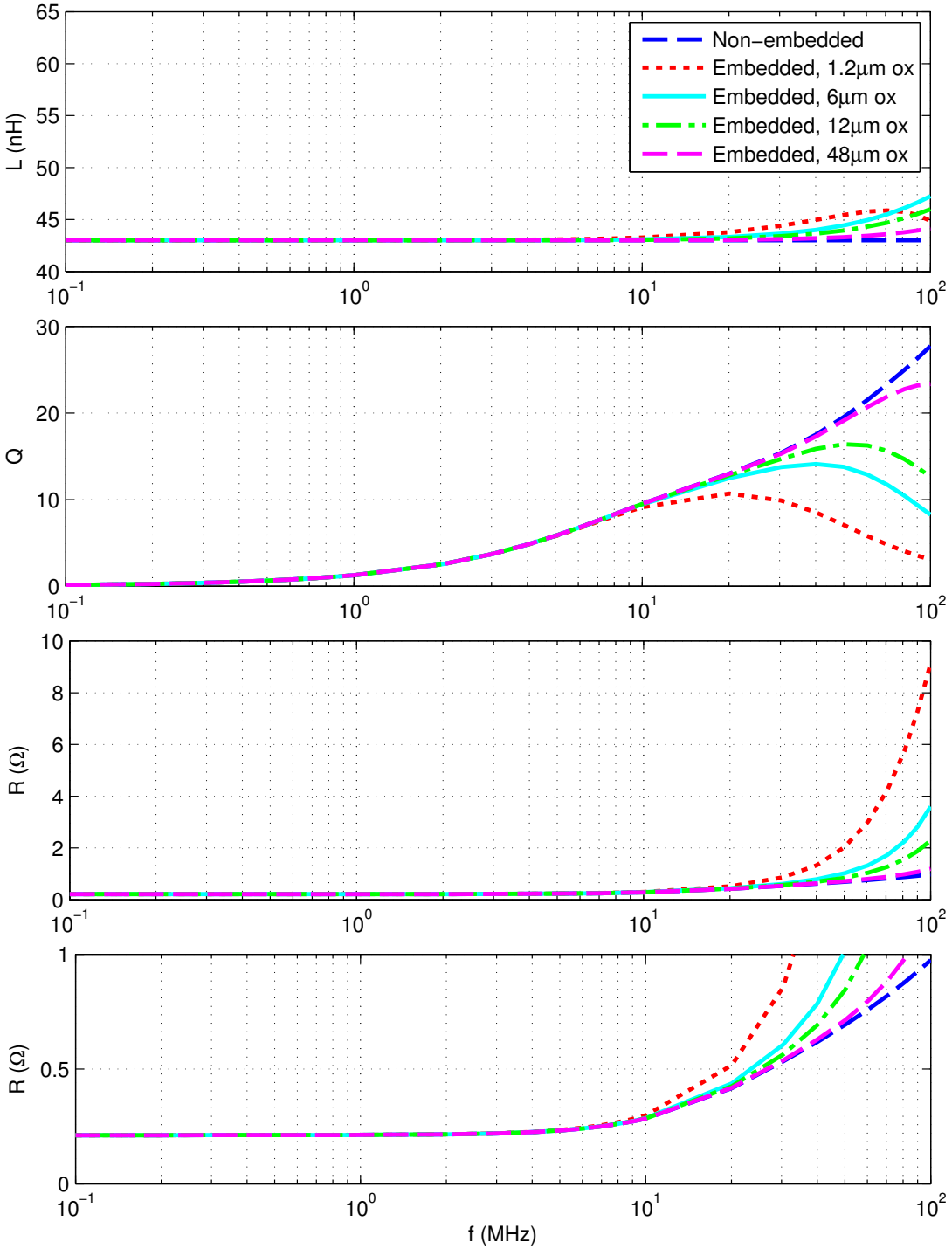


Figure 56: Simulated inductance (L), quality factor (Q) and resistance (R) of the non-embedded and embedded inductors in standard-resistivity (1-30 $\Omega \cdot cm$) silicon substrates that are deposited with different insulation thickness.

diameter of 2 mm, an outer diameter of 6 mm, a copper thickness of 30 μm, and a height of 300 μm. From the simulation results, a thin insulation layer, for example, 1.2 μm, can be observed to induce a considerable amount of loss into the embedded inductor at frequencies above 10 MHz and the inductor exhibits a low resonance frequency of below 100 MHz as well, while a thick insulation layer, for example, 48 μm, only induces a small amount of loss into the inductor at very high frequencies such as above 70 MHz. Obviously, the thicker the insulation, the less lossy the embedded inductor. However, the improvement in the quality factor could reach a saturation after increasing the oxide thickness beyond certain point, as can be seen from Figure 57 that summarizes the simulated quality factors at 50 MHz vs. oxide thicknesses from results in Figure 56. Besides, given fabrication constraints, there is also a limitation on the maximum thickness of the SiO_2 layer that can be deposited using PECVD technology. Therefore, 12 μm is chosen as a practical thickness of the oxide layer. Introducing other insulation materials with lower relative permittivity could also serve as a way to reduce the parasitic capacitance; however, the difficulty in

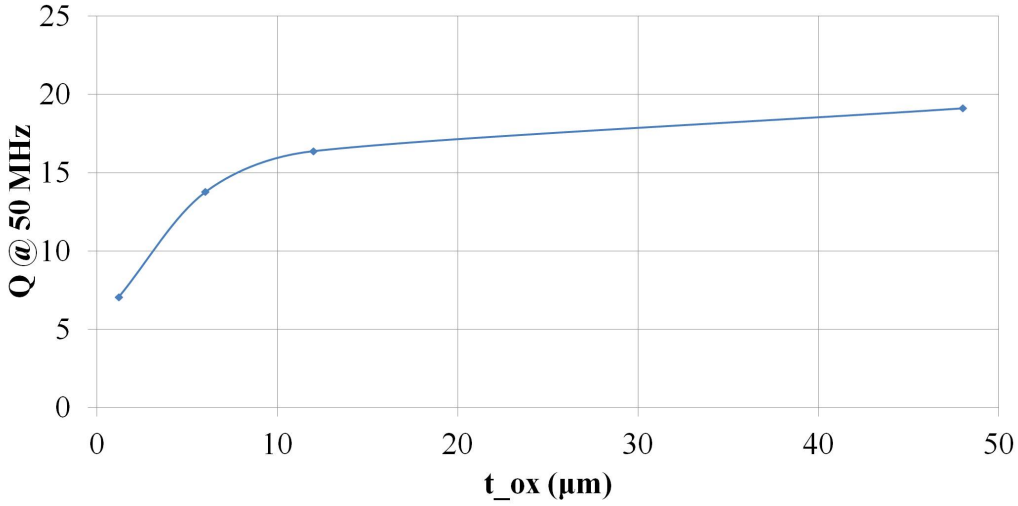


Figure 57: Simulated quality factors (Q) at 50 MHz of the embedded inductors in standard-resistivity (1-30 $\Omega \cdot cm$) silicon wafers passivated with various oxide thicknesses.

integrating other materials into the fabrication process and their compatibility with the CMOS processes needs to be considered.

With an insulation thickness maximized under practical fabrication constraints, the effect of varying parasitic resistance to further reduce the substrate coupling loss is investigated. With the inductor geometry being maintained again the same as before and a fixed oxide thickness of 12 μm, variation of the substrate resistivity is simulated and the results are shown in Figure 58. At frequencies below 30 MHz, the inductor performance is not affected by the substrate resistivity to as low as 1 $\Omega \cdot cm$. However, at higher frequencies, wafers with standard resistivities (1-30 $\Omega \cdot cm$) are found to generate more losses than wafers with higher resistivities such as 500 $\Omega \cdot cm$ and 2000 $\Omega \cdot cm$. Also, the simulated quality factor of the embedded inductor does not increase monolithically with increase of the substrate resistivities, as can be seen from Figure 59 that summarizes the information of simulated quality factors at 100 MHz vs. substrate resistivities from Figure 58. The inductor embedded in 1 $\Omega \cdot cm$ silicon exhibits a higher quality factor than the 500 $\Omega \cdot cm$ case because there is a low-frequency resonance issue in the inductor with the low substrate resistivity of 1 $\Omega \cdot cm$ although they exhibit similar losses. Nonetheless, once passing certain resistivity, the quality factor would increase monolithically with increasing substrate resistivities.

This observation corresponds to the understanding of two extreme cases of having either a zero or an infinite substrate resistivity. When there is a substrate resistivity of zero, there would be no loss coming from the parasitic resistance as there is no parasitic resistance, although there would be current present; when there is a substrate resistivity of infinity, there would be no loss as well since the induced current would be zero although there is parasitic resistance. Therefore, there is a worst case where substrate loss will be the largest at certain resistivity. Care should be taken to avoid selecting the substrate resistivity close to the worst point. Since the simulated

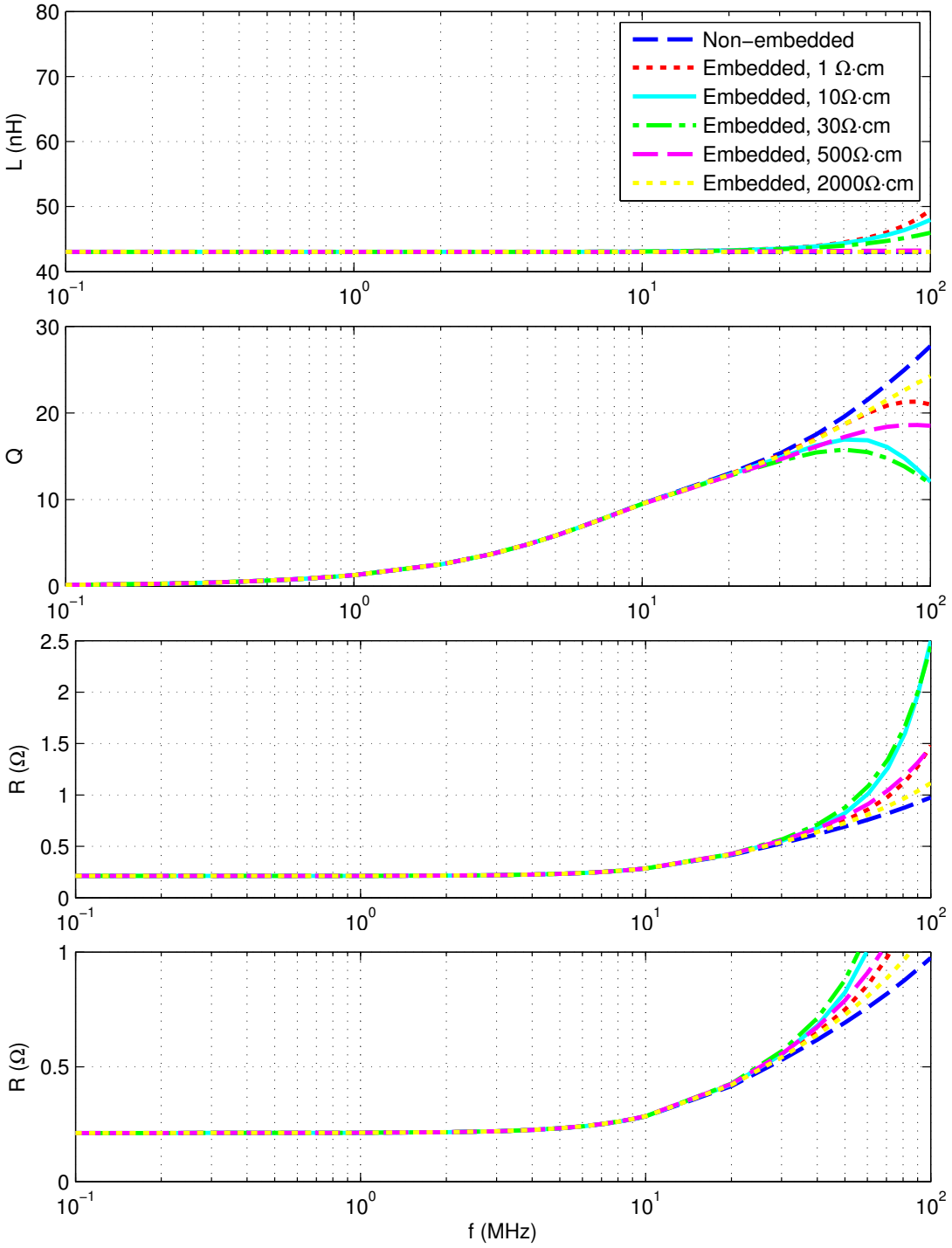


Figure 58: Simulated inductance (L), quality factor (Q) and resistance (R) of the non-embedded and embedded inductors in silicon substrates that possess different resistivities.

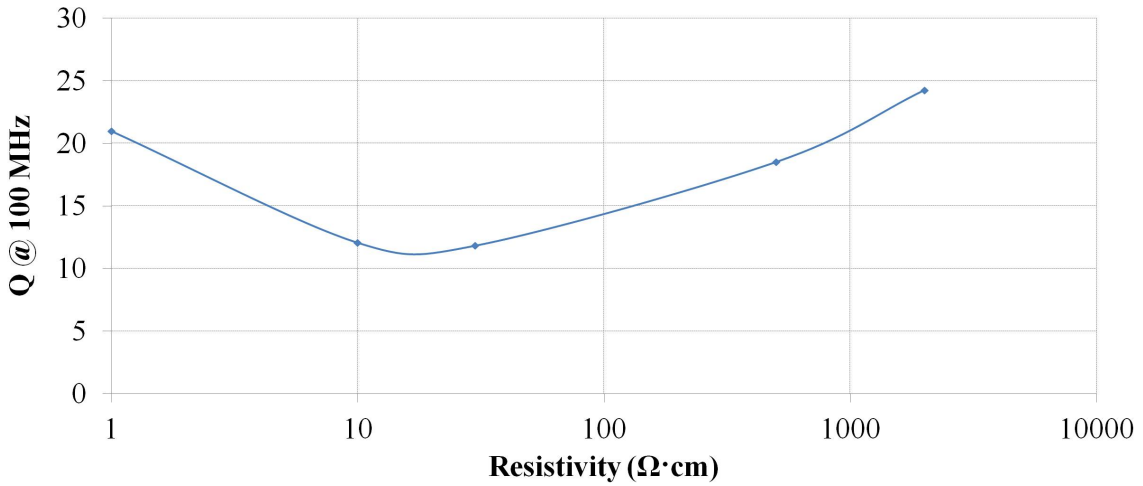


Figure 59: Simulated quality factors (Q) at 100 MHz of the embedded inductors in silicon wafers with various resistivities.

quality factor of the embedded inductor in a substrate with a resistivity of 2000 $\Omega \cdot cm$ approaches that of an inductor without silicon substrate, considering the ready availability of the high-resistivity silicon substrates ranging from 100 $\Omega \cdot cm$ to 10000 $\Omega \cdot cm$ in practice, substrate-associated losses in the embedded inductor can be further suppressed by adopting high-resistivity silicon substrates if necessary.

In conclusion, based on the distributed circuit model that we developed, substrate parasitic losses can significantly degrade the device performance at high frequencies and lower the resonance frequency. Depending on the operating frequency of interest and performance requirements, appropriate handling of the substrate parasitics should be determined.

For our targeted applications operating at 3-30 MHz, the above modeling results suggest that after employing an oxide thickness of 12 μm, the substrate parasitic losses are not significant compared to the copper loss in the embedded inductor. Therefore, the optimization strategy in Regime B should be followed if an initial air-core design is not satisfactory, that is, efforts should be put into optimizing the inductor geometry itself instead of suppressing substrate parasitics in order to improve

the device performance.

4.3.4 Magnetic-Core Embedded Inductors

If the required inductance cannot be achieved with air-core embedded designs under fabrication constraints, or the quality factor of the optimized air-core design is not sufficient at the frequency of interest, as we stated before, magnetic cores can be integrated into the silicon-embedded inductors. The fabrication technology to achieve core integration has already been demonstrated in the chapter about silicon embedding technologies.

Although inductance can be enhanced through core integration, including soft magnetic materials in the embedded inductors may introduce additional core-associated losses. These losses may be exacerbated at high frequencies due to the fact that many magnetic materials become extremely lossy in the megahertz range. Without careful design and optimization, unacceptable core losses could overwhelm the gain in the inductance enhancement. Therefore, appropriate magnetic materials suitable for the targeted frequency must be selected.

Losses in the magnetic materials arise from a variety of causes including hysteresis loss, eddy current loss, and anomalous loss. Integrating magnetic material into the silicon-embedded inductor could also lead to coupling losses since the core will be in close proximity to the windings and the silicon substrate. To minimize the complexity of the design process and eliminate the possible coupling and eddy current losses in the magnetic material, only magnetic cores with high resistivities are considered in our designs. Consequently, hysteresis loss will be the main cause for core-associated loss in the embedded inductor and a less-complex design methodology for the silicon-embedded magnetic-core inductors is enabled.

For a targeted inductance value within a given footprint, our design methodology addresses an inductor with a maximized quality factor based on the trade-offs between

copper loss and core loss.

The inductance and quality factor of an embedded magnetic-core inductor can be calculated from the following equations:

$$L_{core} = L_{air} \cdot \mu_r \cdot \frac{t_{core}}{h} = \frac{\mu_0 N^2 h}{2\pi} \ln \frac{d_o}{d_i} \cdot \mu_r \cdot \frac{t_{core}}{h}, \tag{8}$$

$$Q_{core} = \frac{\omega L_{core}}{R_{Cu} + R_{sub} + R_{core}} \approx \frac{\omega L_{core}}{R_{Cu} + R_{core}}, \tag{9}$$

where μ_r is the relative permeability of the integrated magnetic materials, t_{core} is the thickness of the integrated core, $\frac{t_{core}}{h}$ represents the fraction of the inductor volume comprised of magnetic material assuming that the core has the same lateral dimension as the inductor, and R_{core} is the core-associated loss in the embedded inductor.

Given the targeted inductance value, after determining the permeability and thickness of the magnetic material to be integrated in addition to the winding geometrical parameters as we discussed before for the winding designs, the required number of turns in the cored inductor can be calculated from equation (8). Since a thick insulation layer will also be employed in the embedded magnetic-core inductors, substrate coupling loss (R_{sub}) can be ignored at our frequency of interest based on the modeling results from the air-core inductors. The resistive loss originated from the microfabricated inductor windings (R_{Cu}) is non-negligible. Therefore, the achievable quality factor can then be estimated using equation (9) providing that the copper loss and core loss in the inductor are understood for the calculated number of turns at the frequency of interest.

The hysteresis loss in the magnetic cores (R_{core}) is usually described in terms of Steinmetz parameters, i.e., volumetric power loss density versus peak flux density at different operating frequencies. For commercial magnetic cores, volumetric power loss versus frequency is usually provided in the material technical information. If not, a characterization technique as described in [73] can be utilized to obtain the information or impedance characterization of the cores with wound wires (negligible

resistive loss) can be performed under the desired excitation condition to obtain the core loss.

If the quality factor calculated from equation (9) is not sufficient based on the selected design parameters, analysis of the losses is needed to determine the right optimization strategy in improving the design results. Depending on the significance of different losses, the optimization strategy can be divided into three regimes.

- Regime A: If $R_{Cu} \gg R_{core}$, which is often the case for microfabricated inductors with limited copper thickness working at low frequencies, or with low-permeability magnetic materials, the optimization strategy should be to maximize the core volume and minimize the number of turns to reduce the copper loss.

- Regime B: If $R_{Cu} \ll R_{core}$, which is often the case for core-integrated inductors at high frequencies, or with high-permeability magnetic materials, the core thickness should be reduced with the number of turns increased until a minimum total loss is obtained or core saturation limit is reached. In the cases of having extremely lossy magnetic material, changing the material could be the favorable alternative.

- Regime C: If R_{Cu} is comparable to R_{core}, an optimization should be obtained for a turn number and a core thickness that enables $R_{Cu} + R_{core}$ to be a minimum.

As an example to demonstrate the methodology, silicon-embedded inductors integrating iron powder cores are designed for two different inductances as shown in Table 3. Material mix -2 and -6 from Micrometals [74] are selected due to their stable performance for frequencies up to 100 MHz. These materials have permeability in the range of 8.5-10 and are specially designed to have low losses for operation at tens of megahertz. Since the copper loss is related to the number of turns in the inductor and the core loss can be affected both by the number of turns and the core thickness,

Table 3: Design Results Following the Proposed Design Methodology and Optimization Strategy for Silicon-Embedded Magnetic-Core Inductors

	Design I		Design II	
	Case 1	Case 2	Case 1	Case 2
Design goals				
Targeted inductance (nH)	300	300	600	600
Design parameters				
Inductor height (μm)	300	300	300	300
Inductor outer diameter (mm)	6	6	8	8
Inductor inner diameter (mm)	2	2	3.6	3.6
Core material	-2	-6	-2	-6
Core permeability	10	8.5	10	8.5
Desired core thickness (μm)	250	250	250	250
Design results				
Estimated turn No.	23	25	39	42
Estimated Cu loss (Ω) @10 MHz	0.4	0.4	0.8	0.8
Estimated core loss (Ω) @10 MHz	0.08	0.07	0.32	0.24
Estimated Q @10 MHz	39	40	34	36

the inductor design procedure is actually an iterative process following our design methodology.

First, assuming the core loss is negligible compared to the copper loss at 10 MHz, following the strategy discussed in Regime 1, a maximized core thickness of 250 μm is selected and the number of turns is calculated using equation (8), as shown in Table 3. Second, estimations of the copper loss and core loss at the calculated number of turns are performed and the results are shown in Figure 60. The copper losses are obtained from measurements of fabricated air-core inductors with the desired number of turns wile the core losses are obtained from measurements of the wire-wound inductors with the desired core thickness and number of turns. As can be seen from Figure 60 and summarized in Table 3, at the frequency of 10 MHz, the copper loss is approximately 0.4 Ω for Design I and 0.8 Ω for Design II while the core loss is approximately 0.07-0.08 Ω for Design I and 0.24-0.32 Ω for Design II, depending on

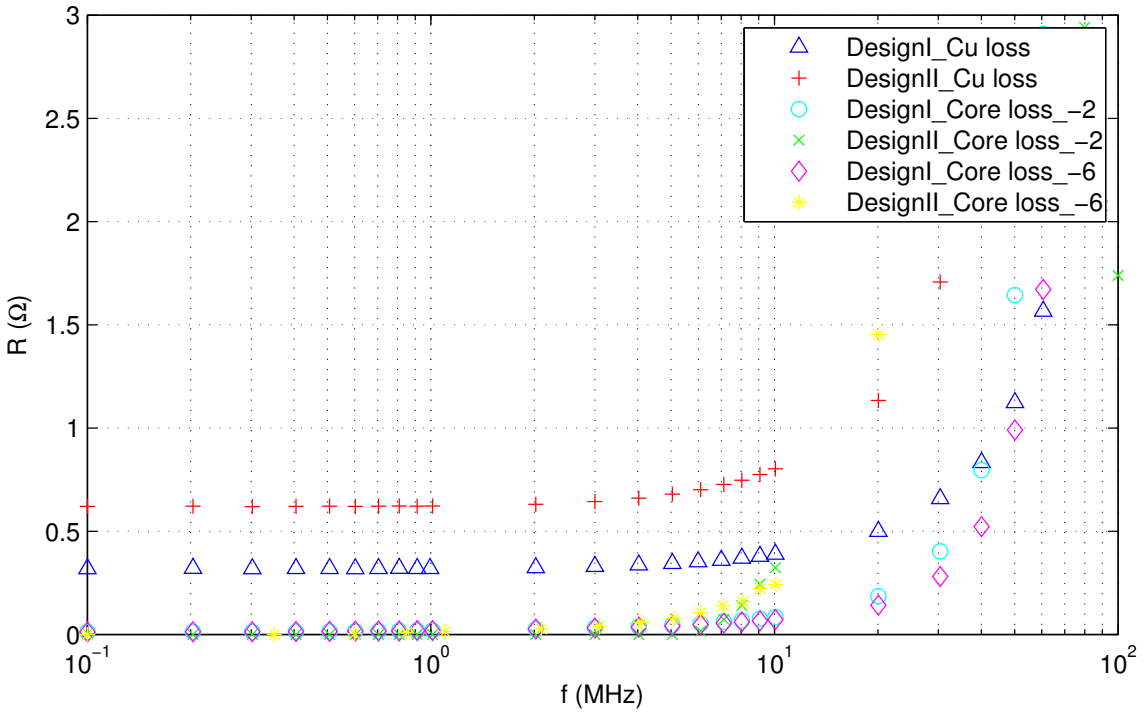


Figure 60: Estimated copper loss in the microfabricated windings and core loss in the magnetic core under low voltage excitation condition.

the materials to be integrated. This verifies our assumption and validates our choice of maximizing the core thickness. Therefore an optimized design has been achieved. The quality factor can then be estimated using equation (9) based on the inductance and the estimated losses, which is also shown in Table 3. If the core loss is estimated to be larger than the copper loss at the calculated number of turns, the core thickness should be reduced and the losses should be re-estimated based on the re-calculated value for the number of turns. This process should be iterated until an optimized or satisfactory design is found, as discussed in Regime 2 and 3.

CHAPTER V

DEVICE CHARACTERIZATION AND TESTING

Testing of the embedded inductors comprises two parts: characterization of the devices themselves and testing of the inductors operating in the targeted power converter circuits. In the following sections, characterization results of the embedded air-core and magnetic-core inductors will first be presented, followed by in-circuit testing results of our inductors.

5.1 Inductor Characterization

The embedded inductors are designed with electroplated pads at the two terminals for measurements. Electrical characterization is performed by probing on the pads of the inductor with two copper pins that are connected to an impedance analyzer (HP4194), as shown in Figure 61. Calibration of the impedance analyzer is performed prior to inductor measurements to eliminate the interference of the interface parasitics on the measurement results, including the interface connector and the copper probes. The

Figure 61: Inductor measurement setup with the impedance analyzer shown on the left and the probe station shown on the right.

inductance and resistance of the device under test is extracted from the imaginary and real part of the measured impedance in the frequency range of 100 kHz to 100 MHz.

In this section, measurements results of the silicon-embedded inductors fabricated based on the various embedding technologies that we have developed will be presented sequentially.

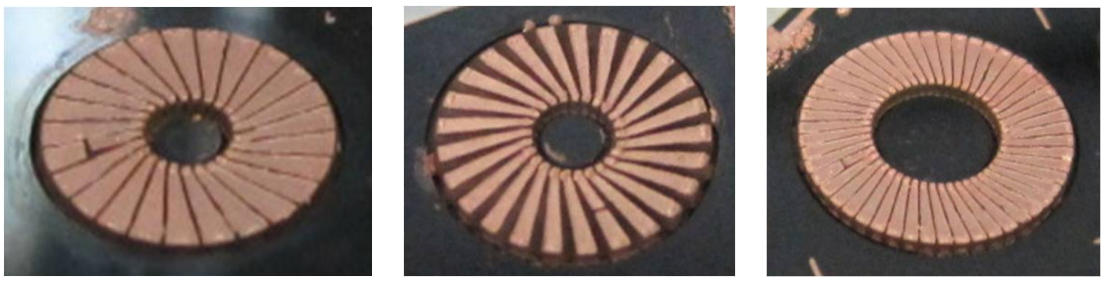
5.1.1 Embedded Air-Core Inductors

5.1.1.1 Lithography-Based Approach

There are three inductor designs that have been fabricated using the lithography-based approach, as shown in Figure 62. The details of their geometries are as follows.

Design I has 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 350-450 μm, a constant gap of 100 μm between adjacent windings, a copper thickness of 20-25 μm, and is embedded in a 300-μm-deep trench in standard-resistivity (1-30 $\Omega \cdot cm$) silicon that is passivated with a 6-μm-thick oxide layer. Measurement results of the fabricated design I inductors are shown in Figure 63. Inductances of 43-45 nH and maximum quality factors of 5-6 are achieved for these inductors.

Design II has 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a



(a) (b) (c)

Figure 62: Fabricated three embedded inductor designs: (a) design I, (b) design II, and (c) design III.

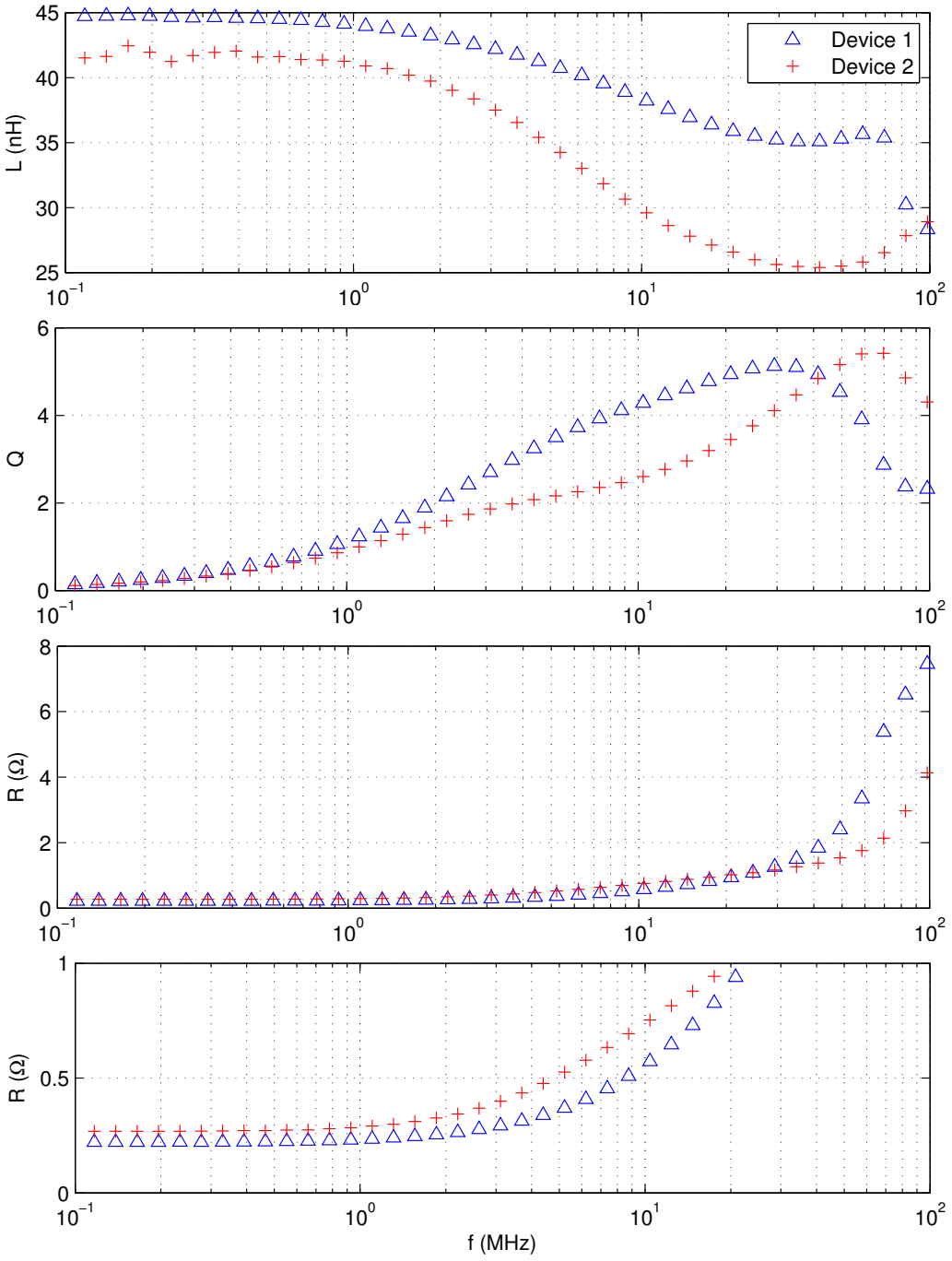


Figure 63: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the embedded inductor design I fabricated using the lithography-based approach. Device 1 and Device 2 denotes two inductors of nominally identical design as described in the text.

height of approximately 400 μm, a gap equal to the winding width, a copper thickness of 20-25 μm, and is embedded in a 300-μm-deep trench in standard-resistivity (1-30 $\Omega \cdot cm$) silicon that is passivated with a 6-μm-thick oxide layer. Measurement results of the fabricated inductor using the lithography-based approach are shown in Figure 64 and compared to an inductor that is also partially released in the trench. An inductance of approximately 60 nH, a DC resistance of 400 $m\Omega$ and a quality factor of 4.5 at 10 MHz is measured for the unreleased inductor.

Note that this batch of the fabricated inductors does not have a thick insulation layer as suggested by the modeling results. Therefore, substrate parasitics might have a detrimental effect on the inductor performance at high frequencies.

Partial release of the embedded inductor is conducted to confirm the parasitic coupling effect between the embedded windings and the substrate. The partial release is achieved through performing an abrupt heating and cooling cycle on the embedded inductor such that the inductor is still embedded in the silicon trench, yet an air gap is introduced between some of the bottom radial windings and the silicon substrate due to partial delamination of the inductor body from the silicon trench. Consequently, the parasitic capacitance due to winding-to-substrate proximity is reduced. The measured inductor quality factor improves to 17.5 at approximately 70 MHz from the original 4.5 at approximately 10 MHz, suggesting that the coupling effect has been reduced at high frequencies.

Upon verifying the significance of the substrate parasitic coupling through thin insulation layers, a 12-μm-thick oxide layer is employed for inductor design III that is fabricated subsequently. Design III has 50 turns, an inner diameter of 4 mm, an outer diameter of 8 mm, a height of 350-400 μm, a constant gap of 100 μm, a copper thickness of 20-25 μm, and is embedded in a 300-μm-deep trench in standard-resistivity (1-30 $\Omega \cdot cm$) silicon. Measurement results of the fabricated inductors are shown in Figure 65. Inductances of 103-121 nH and quality factors of 13-16 are

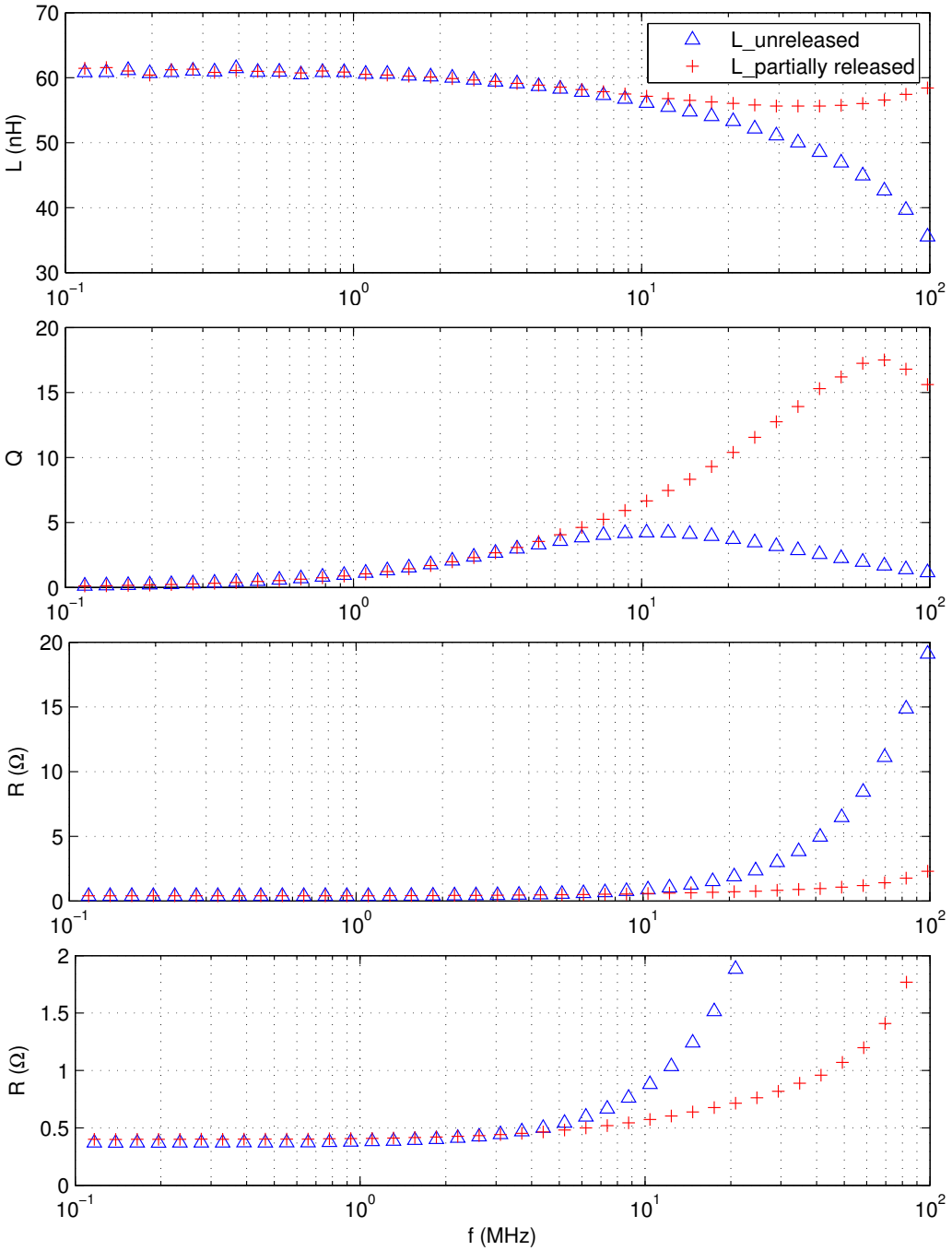


Figure 64: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the embedded inductor design II fabricated using the lithography-based approach.

achieved around 40-50 MHz.

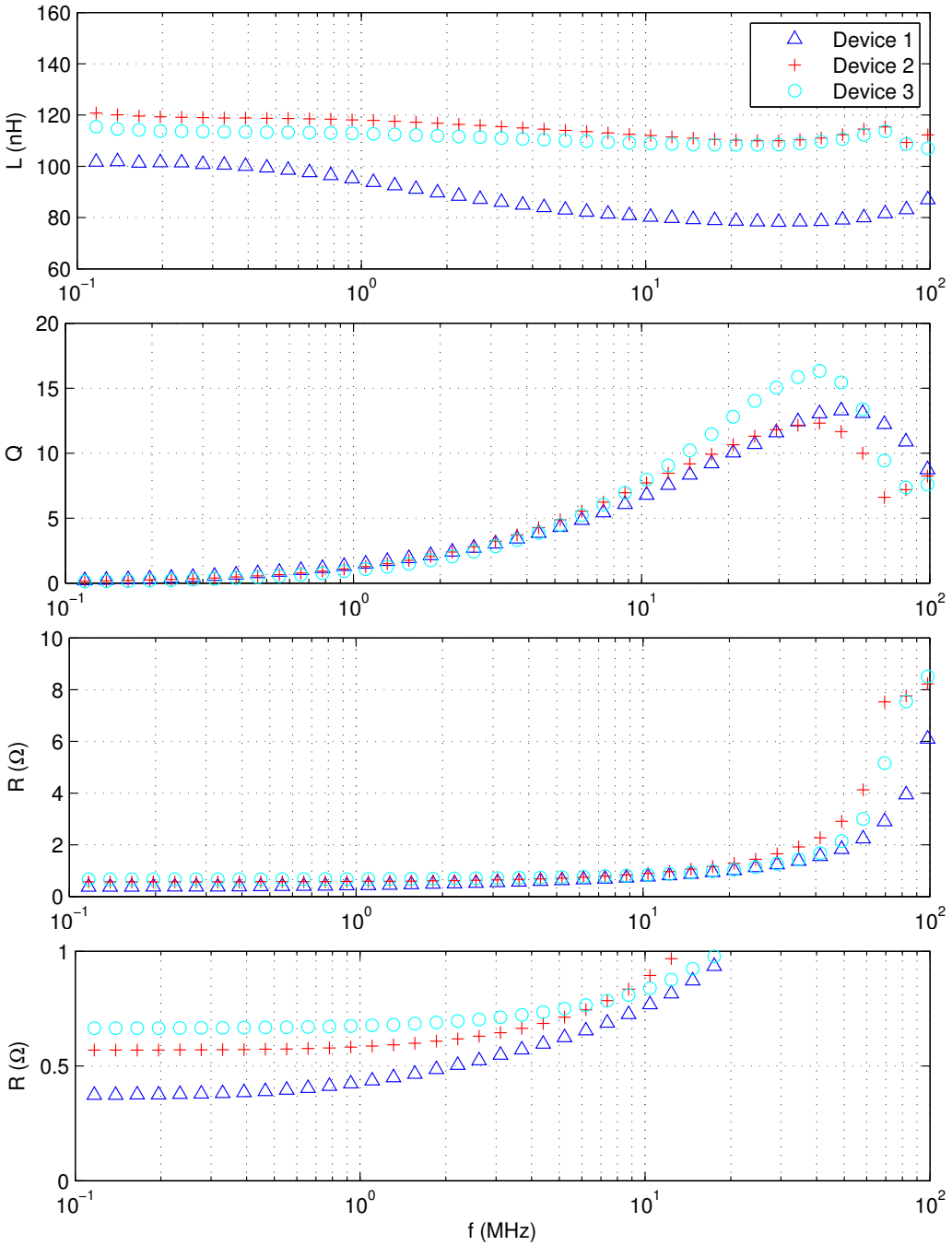


Figure 65: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the embedded inductor design III fabricated using the lithography-based approach. Device 1-3 denote three inductors of nominally identical design as described in the text.

5.1.1.2 Through-Wafer Interconnects

The integration of through-wafer interconnects with embedded inductors is also demonstrated using the lithography-based approach as an example. The fabricated inductor

design III demonstrates an inductance of 110 nH and a DC resistance of 1.3 Ω, as shown in Figure 66. The achieved quality factor is low partially because the substrate is passivated only with a thin insulation layer. Another reason is that the process for fabricating the through-wafer interconnects is not optimized in this device, consequently the electroplated copper in the through-silicon vias is thin (20 μm), which adds a large resistance to the embedded device and therefore degrades its quality factor.

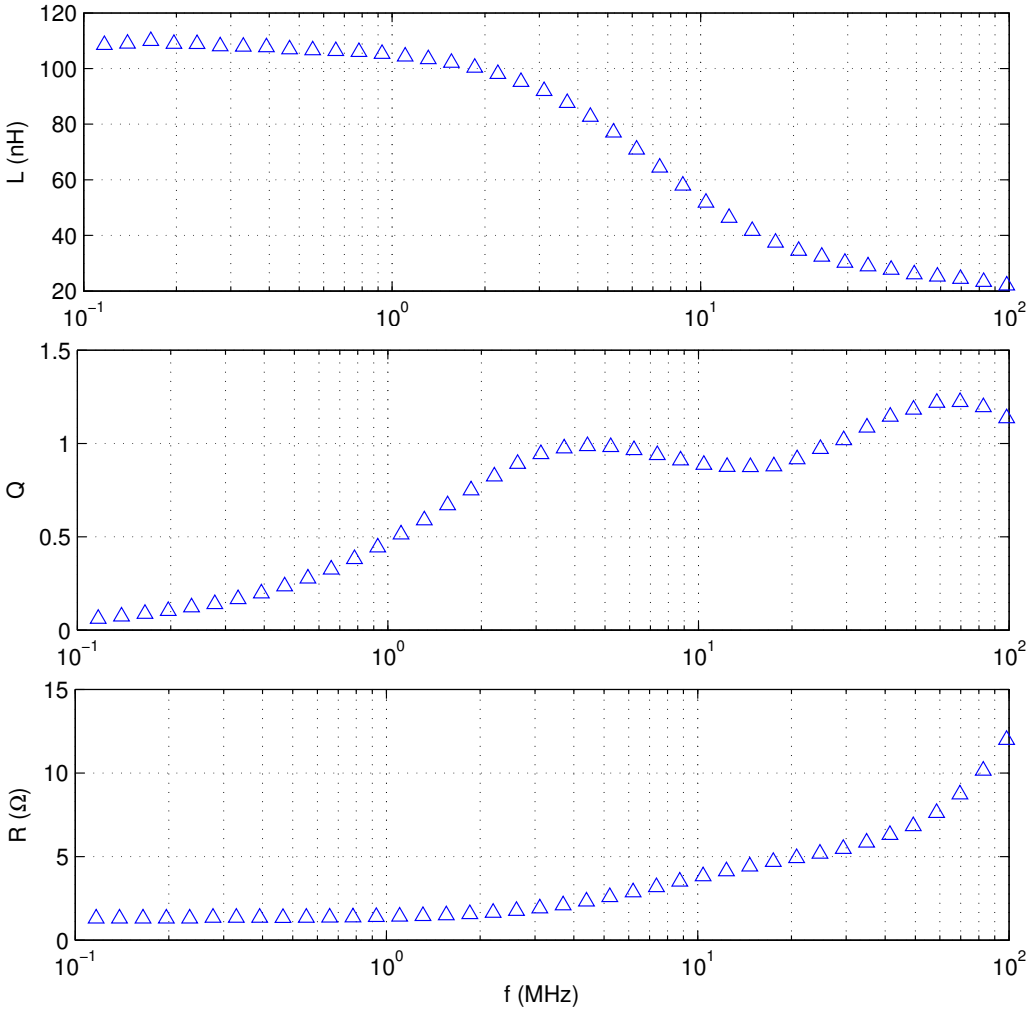


Figure 66: Measured inductance (L), quality factor (Q), and resistance (R) of the embedded inductor design III with through-wafer interconnect using the lithography-based approach.

5.1.1.3 Shadow Mask-Based Approach

Characterization results of the silicon-embedded inductors fabricated using the 3-D shadow-mask approach are shown in Figure 67, 68, and 69.

The fabricated inductor design I shown in Figure 67 has 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, a winding gap of 100 μm, a copper thickness of approximate 30 μm and a 12-μm-thick oxide layer on a standard-resistivity (1-30 $\Omega \cdot cm$) silicon. The characterization results demonstrate an overall inductance of 43-46 nH, a DC resistance of 290 $m\Omega$, and a quality factor of 16 at 40 MHz. These inductors exhibit a lower inductance than those fabricated using the lithography-based approach because they have a smaller height due to the fact that their top conductors are maintained coplanar with the substrate surface. The quality factor of these devices is improved significantly over the measured value of 4.5 for the unreleased inductor with a thin insulation layer using the lithography-based approach, demonstrating again the importance of parasitics suppressing.

Design II has 50 turns, an inner diameter of 4 mm, an outer diameter of 8 mm, a height of approximate 300 μm, a winding gap of 100 μm, and a copper thickness of approximate 30 μm with a 12-μm-thick oxide layer on a standard-resistivity (1-30 $\Omega \cdot cm$) silicon substrate. An inductance in the range of 86-97 nH and a quality factor of 8-10 is obtained for these devices as shown in Figure 68. The demonstrated inductance and quality factor is lower than expected due to some shorts that are found between the windings in the fabricated inductors. Since these inductors have a larger number of turns and a narrower winding width, patterning imperfections tend to happen more, causing shorts in the devices.

Design I inductors are also fabricated using high-resistivity (2000-3000 $\Omega \cdot cm$) wafers and the characterization results are shown in Figure 69. An inductance of 41-53 nH and a quality factor of 15-21 are achieved for these inductors. Note that the quality factor of these inductors increases monolithically with frequency and reaches

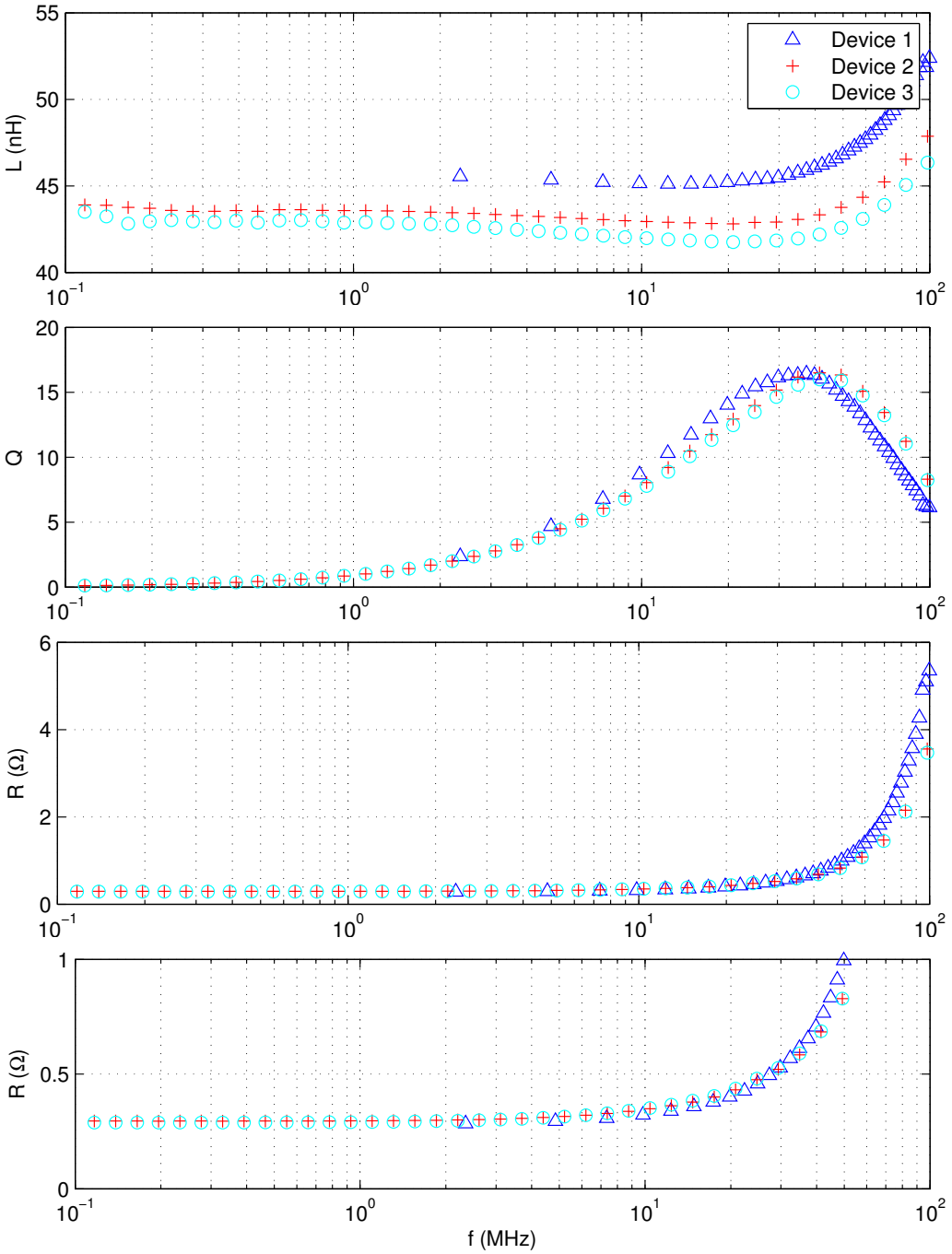


Figure 67: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the embedded toroidal inductor design I using the 3-D shadow mask-based approach. Device 1-3 denote three inductors of nominally identical design as described in the text.

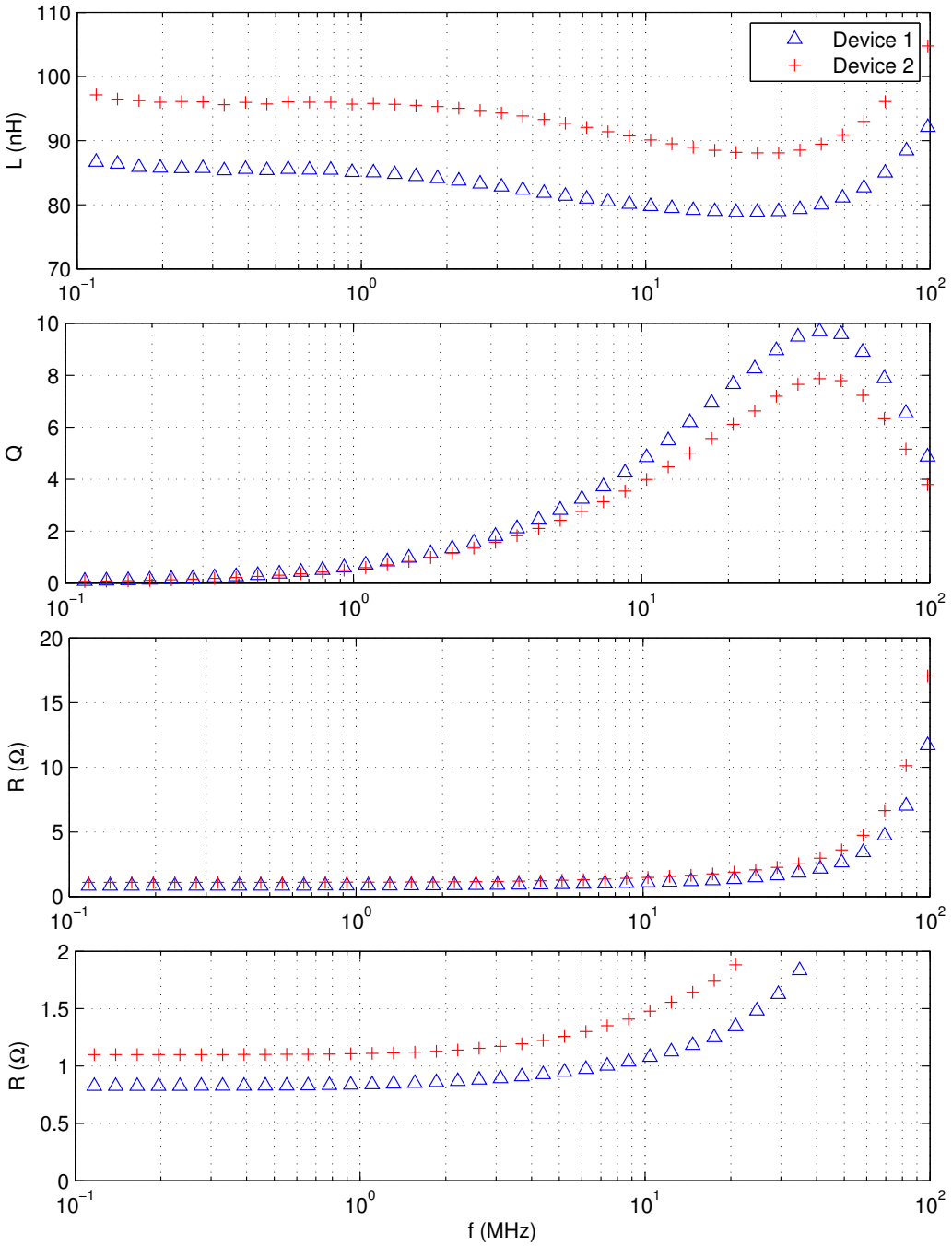


Figure 68: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the embedded toroidal inductor design II using the 3-D shadow mask-based approach. Device 1 and 2 denote two inductors of nominally identical design as described in the text.

maxmimum at 100 MHz, which suggests that the use of high-resistivity substrates suppresses the substrate losses at high frequencies and therefore leads to a higher

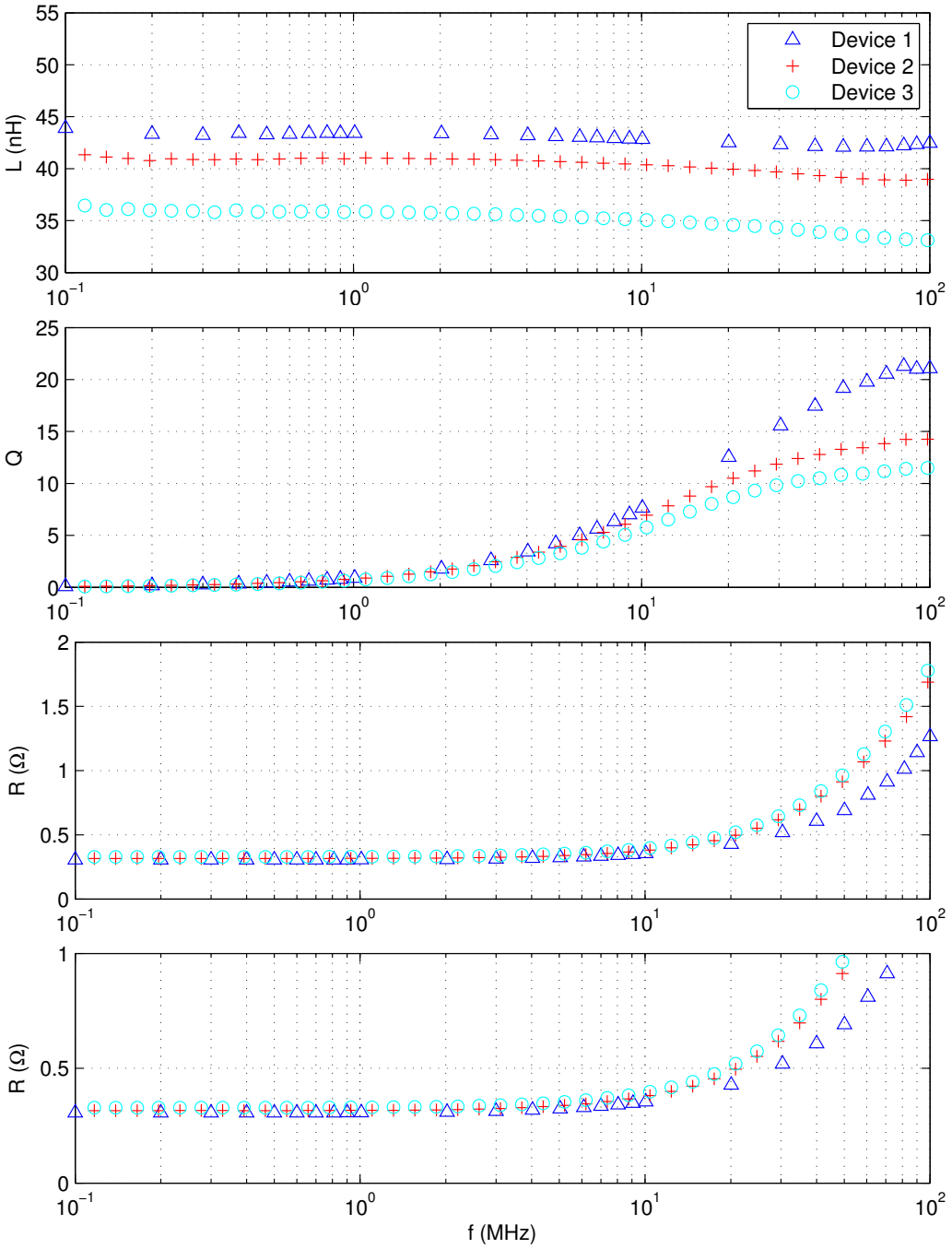


Figure 69: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the toroidal inductor design I embedded in high-resistivity (2000-3000 $\Omega \cdot cm$) silicon using the 3-D shadow mask-based approach. Device 1-3 denote three inductors of nominally identical design as described in the text.

quality factor at higher frequencies. The measured inductance of these inductors is also stable over the entire frequency range, while that of the inductors embedded in standard-resistivity wafers begins to fall and then increase at frequencies close to 100 MHz, suggesting the approaching of a resonance.

5.1.1.4 Inductor Model Validation

To verify the equivalent circuit model that we proposed for the silicon-embedded inductors, inductors that are embedded in standard-resistivity (1-30 $\Omega \cdot cm$, SR embedded inductors) wafers, high-resistivity (2000-3000 $\Omega \cdot cm$, HR embedded inductors) wafers, as well as on glass substrates (non-embedded inductors), are modeled and compared with the experimental results in this section.

To validate modeling of the copper loss in the inductor windings using Dowell's method, non-embedded inductors with various geometries are first fabricated on glass substrates using lithography-based approaches [75] and their characterization results are shown in Figure 70. Since glass substrates do not introduce any silicon-related losses, the measured inductor loss (R) denotes solely the copper loss in the inductor windings.

Among the fabricated on-glass inductors, device 1 possesses 50 turns, an inner diameter of 4 mm, an outer diameter of 8 mm, a height of 600 μm, a copper thickness of 30 μm and a winding gap of 100 μm; device 2 possesses 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 600 μm, a copper thickness of 30 μm and a winding gap of 100 μm; device 3 possesses the same geometry as device 2 except that it has a smaller height of 500 μm.

Modeling of the copper losses in these inductors are performed and the results are compared with the fabricated on-glass inductors, as shown in Figure 71. As can be seen from the figure, Dowell's method gives a reasonable estimation of the frequency-dependent resistance of the inductors for various designs.

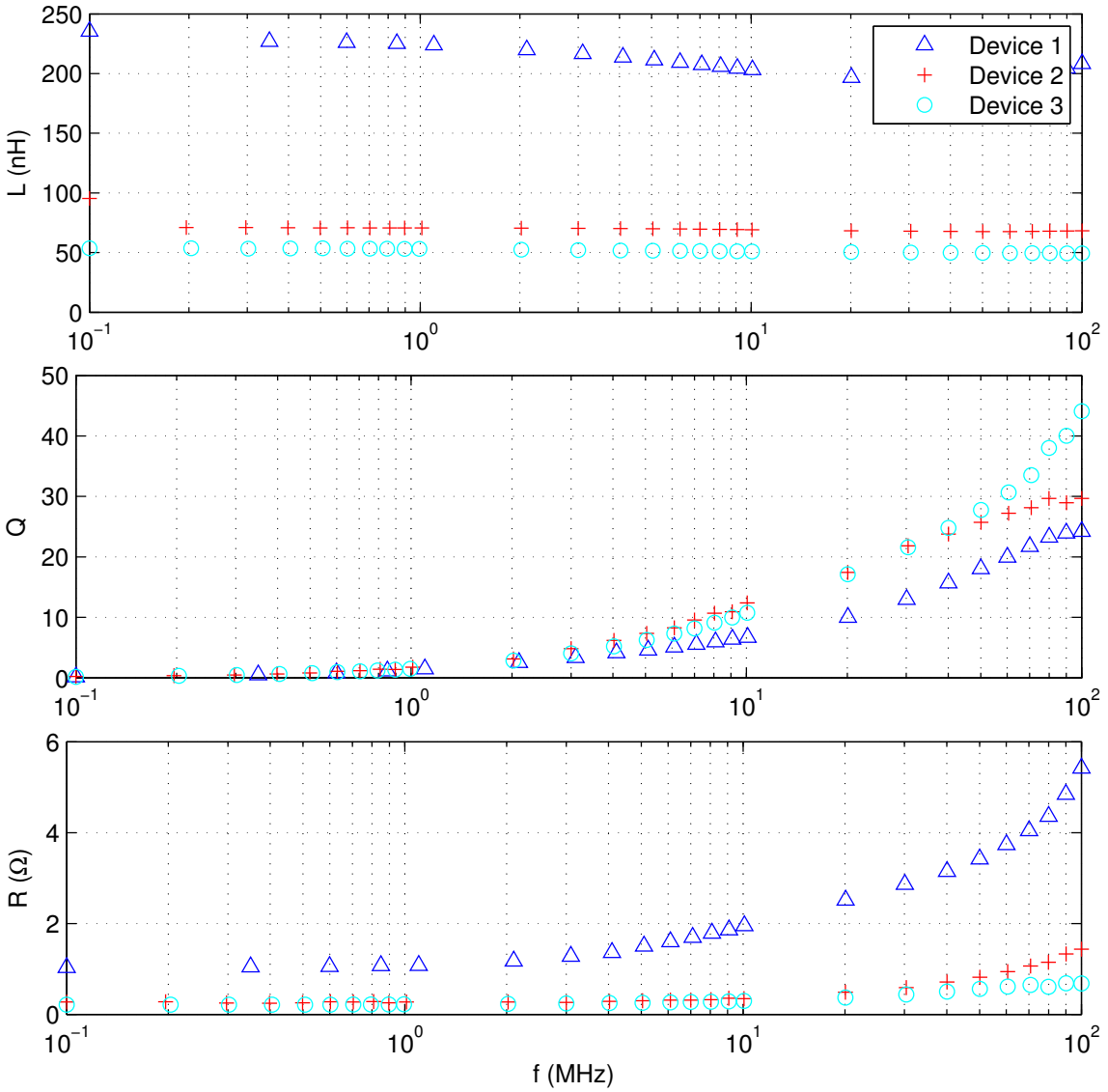


Figure 70: Measured inductance (L), quality factor (Q) and resistance (R) of toroidal inductors with various geometries that are fabricated on glass substrates using lithography-based approaches.

Based on the copper loss model and the proposed circuit model, circuit simulations are performed for inductors embedded in standard-resistivity and high-resistivity wafers, and the results are compared with the experimental results that have been presented before, as shown in Figure 72. Obviously, the modeling results for the non-embedded, SR-embedded(SR stands for standard resistivity) and HR-embedded (HR stands for high resistivity) inductors are in agreement with the experimental results.

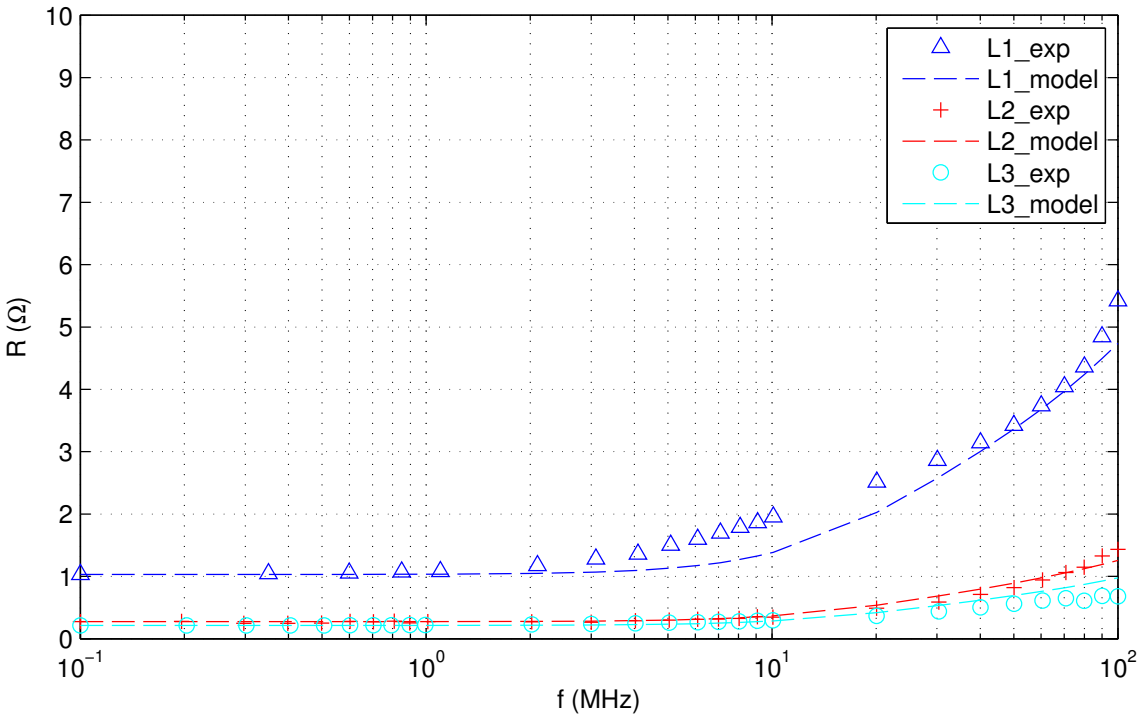


Figure 71: Simulated resistance(lines) and measured resistance (symbols) of the fabricated on-glass toroidal inductors.

In addition, as also indicated by the measured resistances of inductors embedded in different substrates, the loss components in the embedded inductor can vary dramatically at different frequencies of interest. The SR-embedded inductor suffers from large parasitic coupling losses at frequencies above 50 MHz while the coupling loss in HR-embedded inductors are suppressed effectively. In comparison to the non-embedded inductor that achieved a quality factor of 45 at 100 MHz, the quality factor of the SR-embedded inductor reached a maximum of 16 at 40 MHz and the quality factor of the HR-embedded inductor increased monolithically to 22 at 100 MHz.

To gain more insights into the loss distribution in the embedded inductor, the losses are decomposed into the copper loss and the silicon loss (that is, the substrate coupling loss) respectively and are plotted against frequency, as shown in Figure 73. The experimental copper loss in the inductor windings is taken to be the characterized resistance of the non-embedded inductor (the difference between the copper loss with

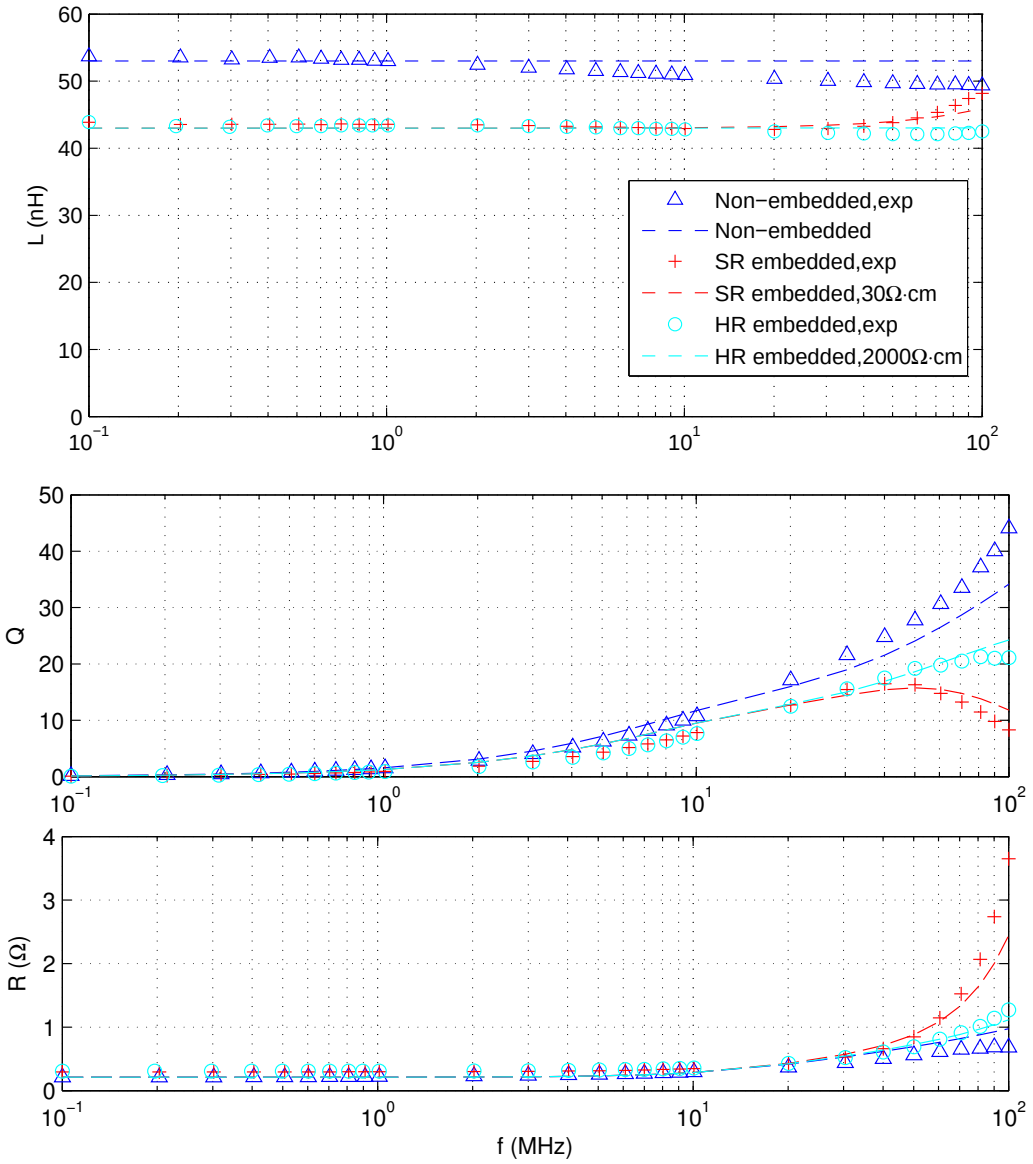


Figure 72: Measured inductance (L), quality factor (Q) and resistance (R) (symbols) of the non-embedded, SR-embedded (1-30 $\Omega \cdot cm$) and HR-embedded (2000-3000 $\Omega \cdot cm$) inductors vs. modeling results (lines).

and without silicon embedding is believed to be small and therefore is ignored here); the experimental silicon loss for the inductors embedded in different silicon substrates is then calculated by subtracting the copper loss from the measured resistance of the silicon-embedded inductors. The simulated copper loss in the inductor windings was taken from Dowell's model; the simulated silicon loss was obtained by subtracting

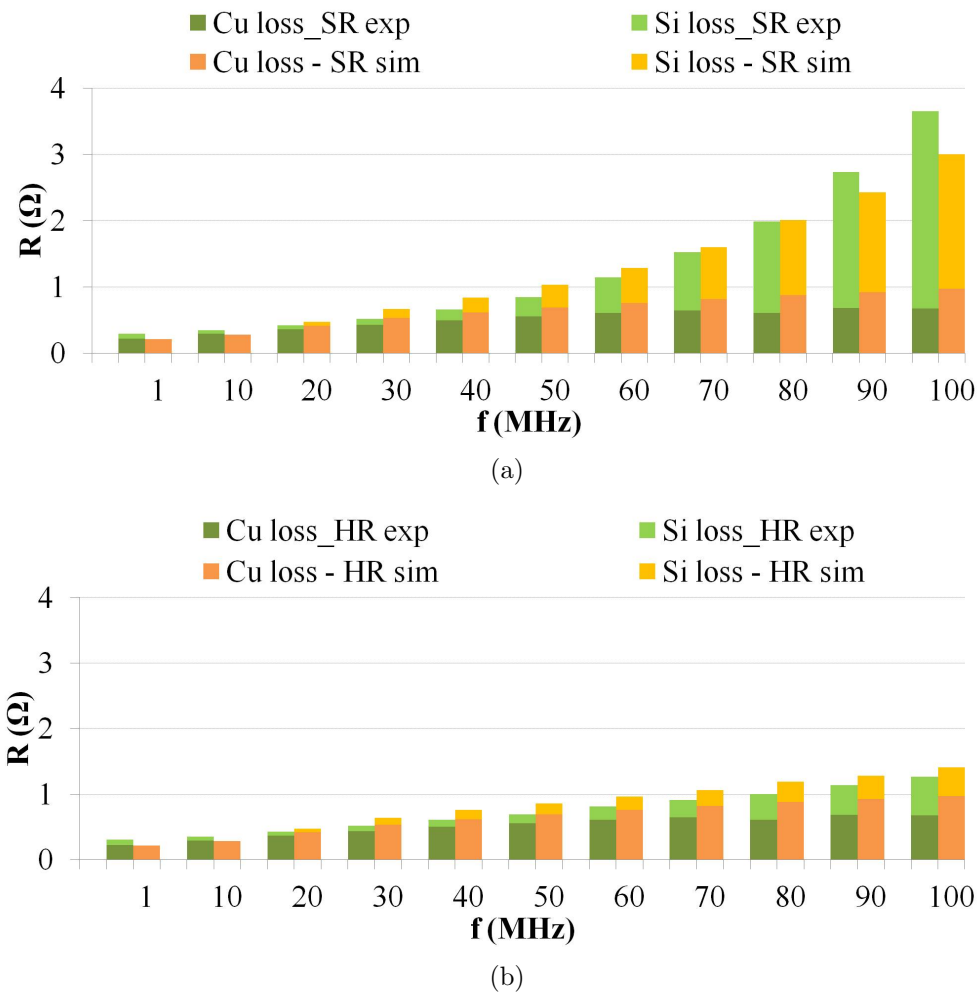


Figure 73: Measured and simulated copper loss and silicon loss of the embedded inductors within standard-resistivity(SR) and high-resistivity(HR) wafers respectively.

the simulated copper loss from the total inductor loss calculated from the equivalent circuit model.

As can be seen from Figure 73, for the SR-embedded inductor, the loss distribution demonstrates that at frequencies below 50 MHz, the silicon loss is negligible compared to the copper loss, suggesting that inductor optimization is more important than wafer resistivity control in terms of improving the device performance. At frequencies above 50 MHz, the silicon loss increases quickly and become comparable to the copper loss at 70 MHz and dominant above 80 MHz, suggesting that the substrate loss

suppression is the key to improve the inductor performance at these frequencies. With the experimental and simulated loss distribution in the HR-embedded inductor, the effectiveness of using high-resistivity substrate to reduce the silicon coupling loss is validated as silicon loss is kept low for the entire range of our frequency of interest.

5.1.1.5 Double-Layer Winding Inductors

Characterization results of the silicon-embedded inductors fabricated with double-layer windings are shown in Figure 74. The fabricated inductor has 24 turns of double-layer windings, which equals a total turn number of 48, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, a winding gap equal to the winding width, a copper thickness of approximate 20 μm and a 12-μm-thick oxide layer on a standard-resistivity (1-30 $\Omega \cdot cm$) silicon.

An inductance of 125-150 nH and a quality factor of 4 is achieved for the fabricated inductors. Obviously, compared to the same design with single-layer windings in the section of shadow mask-based approach (design I), the inductance provided in the same footprint is increased by a factor of 4. However, due to the narrower conductors that are fabricated in the double-layer windings and the non-optimized process that results in a thinner copper to be electroplated, the resistance of these inductors is larger as compared to the device with single-layer windings, which leads to a lowered quality factor. To improve it, wider winding width and thicker copper can be electroplated.

5.1.1.6 Summary

A summary of the characterization results of silicon-embedded inductors is shown in Figure 75. As labeled in the legend, LT stands for the lithography-based approach. SM stands for the shadow mask-based approach. HR stands for high resistivity. DL stands for double-layer winding inductors. From the results, we can see that, single-layer inductors with the same designs using lithography-based approach and shadow

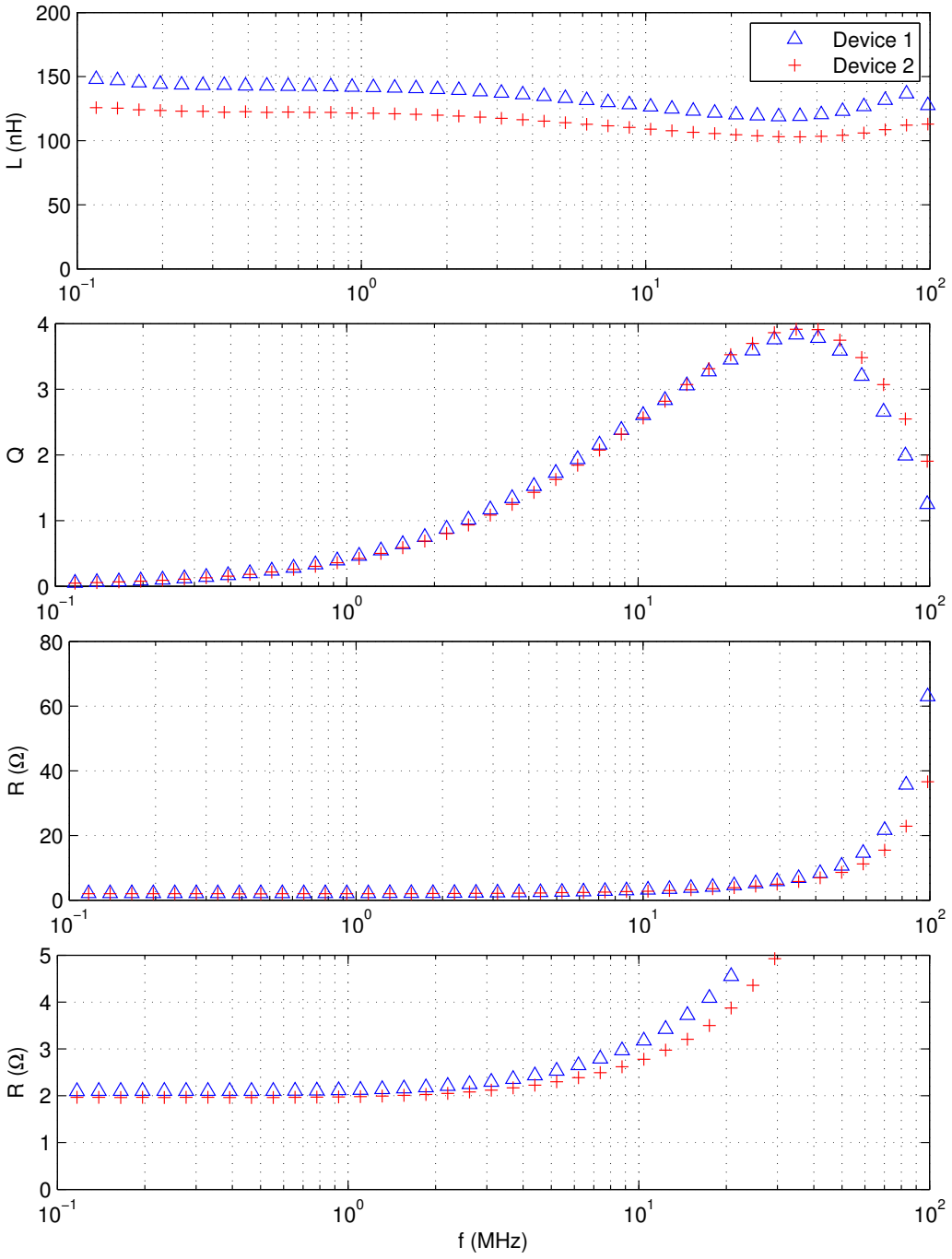


Figure 74: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the fabricated embedded inductor with double-layer windings. Device 1 and 2 denote two inductors of nominally identical design as described in the text.

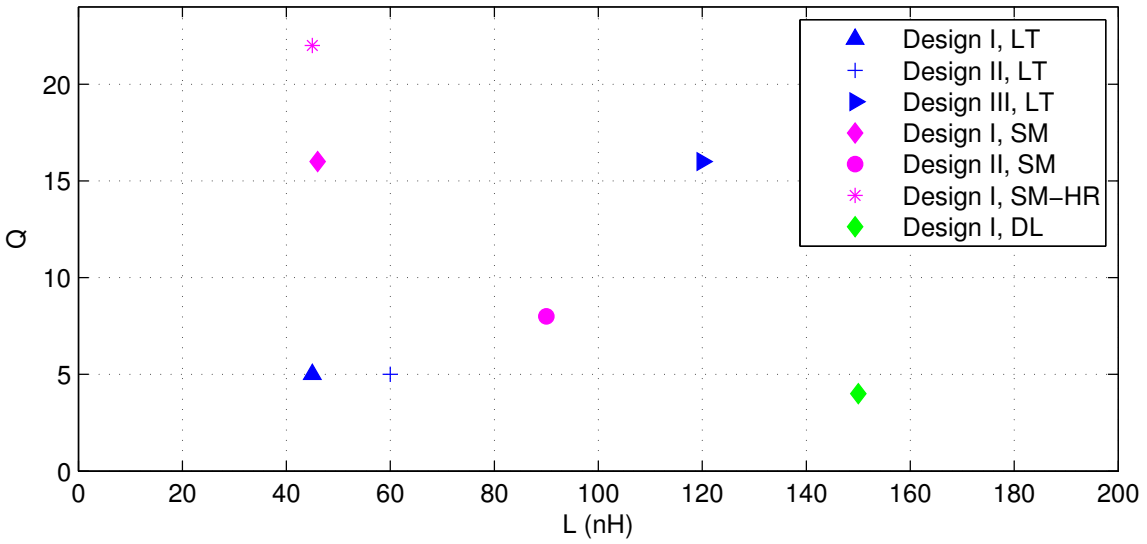


Figure 75: Summary of the fabricated silicon-embedded toridal inductors using different approaches.

mask-based approach demonstrate similar performances. The embedded inductor with double-layer windings demonstrates as expected an inductance of approximately four times the inductance of the single-layer inductors with identical footprint and height. This inductance is also larger than that of the single-layer designs possessing the same number of turns in a larger footprint. However, the quality factor of the double-layer designs is smaller than the single-layer designs due to the reduced widths of the double-layer windings and the non-optimized fabrication process that results in a smaller copper thickness in the device.

5.1.2 Magnetic-Core Inductors

5.1.2.1 Design Methodology Validation

To demonstrate the methodology presented in the section of "Magnetic-Core Embedded Inductor", silicon-embedded inductors integrating iron powder cores are fabricated according to the design results of the presented example in that section, and their characterization results are shown in Figure 76 with key information also summarized in Table 4.

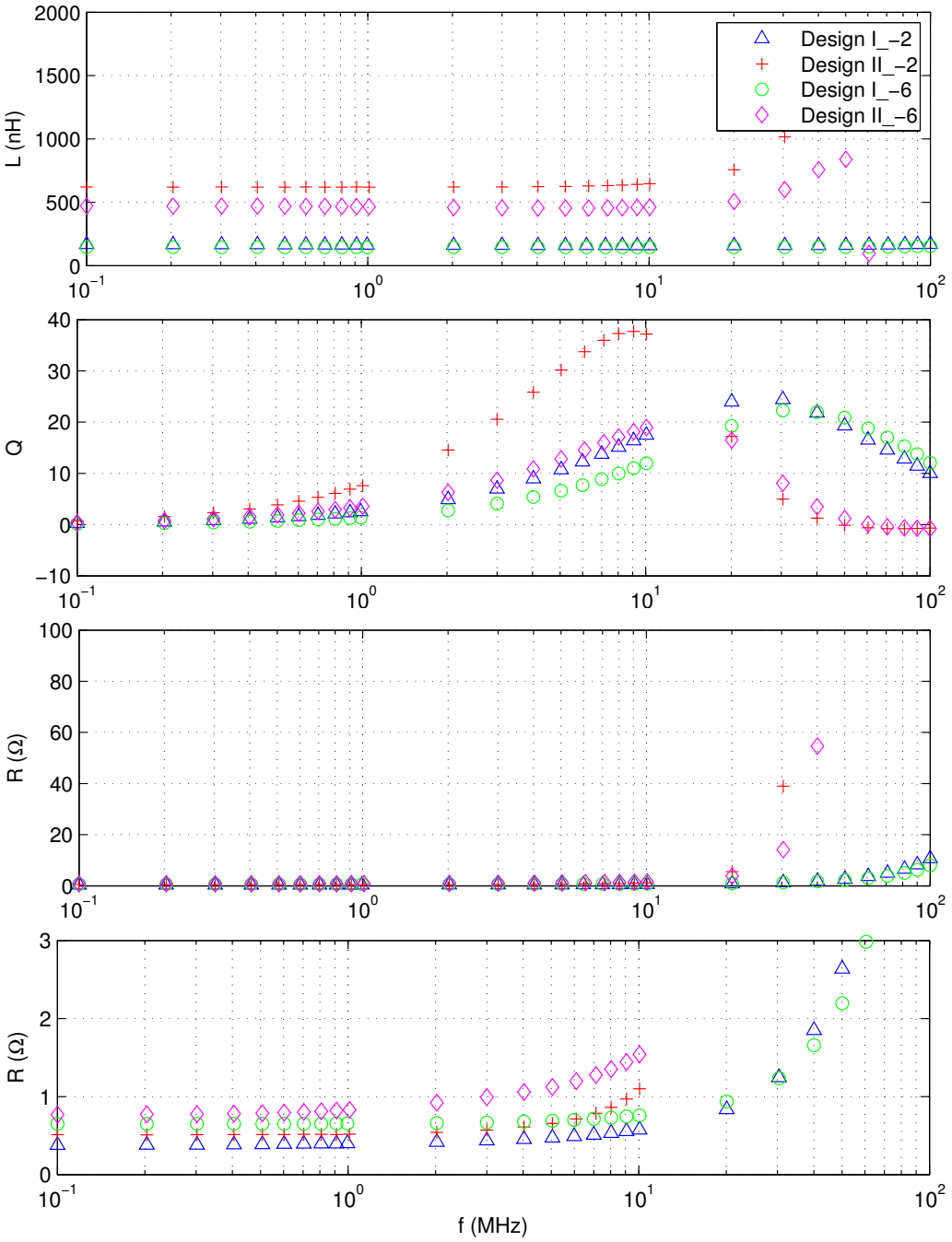


Figure 76: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with iron powder cores.

For inductors fabricated following Design I, since the integrated iron powder cores have a nonmagnetic factory-coated passivation layer of approximately 100 μm in

Table 4: Optimized Inductor Designs Integrating Iron Powders Cores and Fabrication Results

	Design I		Design II	
	Case 1	Case 2	Case 1	Case 2
Design goals				
Targeted inductance (nH)	300	300	600	600
Design parameters				
Inductor height (μm)	300	300	300	300
Inductor outer diameter (mm)	6	6	8	8
Inductor inner diameter (mm)	2	2	3.6	3.6
Core material	-2	-6	-2	-6
Core permeability	10	8.5	10	8.5
Desired core thickness (μm)	250	250	250	250
Design results				
Estimated turn No.	23	25	39	42
Estimated Cu loss (Ω) @10 MHz	0.4	0.4	0.8	0.8
Estimated core loss (Ω) @10 MHz	0.08	0.07	0.32	0.24
Estimated Q @10 MHz	39	40	34	36
Fabrication results				
Integrated core thickness (μm)	150	150	250	230
Fabricated turn No.	25	25	40	40
Calculated inductance (nH)	188	159	607	475
Estimated Q @10MHz	17	15	34	29
Measured inductance (nH)	167	140	620	470
Measured total loss (Ω) @10 MHz	0.58	0.75	1.1	1.5
Measured Q @10 MHz	17.5	12	37	19

thickness, the resulted effective core thickness in the fabricated inductors is only 150 μm, preventing the inductor from achieving the optimized design results. Besides, the lateral dimension of the cores is also approximately 30% smaller than the inductor lateral dimension. However, they do show results consistent with our design methodology considering the effective dimension of the integrated cores.

For inductors fabricated following Design II, the cores are lapped on both sides to make sure the desired thicknesses are integrated into the inductors. As a result, it can be seen from the table that measurement results of the fabricated devices match well

with the optimized design results. The device integrating material -2 demonstrated an inductance of 620 nH and a high quality factor of 37 at 10 MHz, which meets the circuit requirements of our targeted applications. In conclusion, the methodology is shown to guide the inductor design procedure well to generate consistent results in fabrication.

5.1.2.2 Iron Powder Cores

To further improve the performance of the optimized inductor designs integrating iron powder cores (Design II as presented in the previous section), the copper thickness, inductor height, and core thickness in the device is further increased. Images of the fabricated devices are shown in Figure 77 with their characterization results shown in Figure 78 and 79 for devices integrating materials -2 and -6 respectively.

The fabricated inductors in Figure 78 have 40 turns, an inner diameter of 3.6 mm, an outer diameter of 8 mm, a height of 300 μm and an increased copper thickness of approximate 50 μm. The iron powder cores have an inner diameter of 3.84 mm, an outer diameter of 7.8 mm, and a thickness of 200-250 μm. The fabricated inductors in Figure 79 have the same geometry as those in Figure 78 except an increased height of

Figure 77: Fabricated silicon-embedded inductors with iron powder cores.

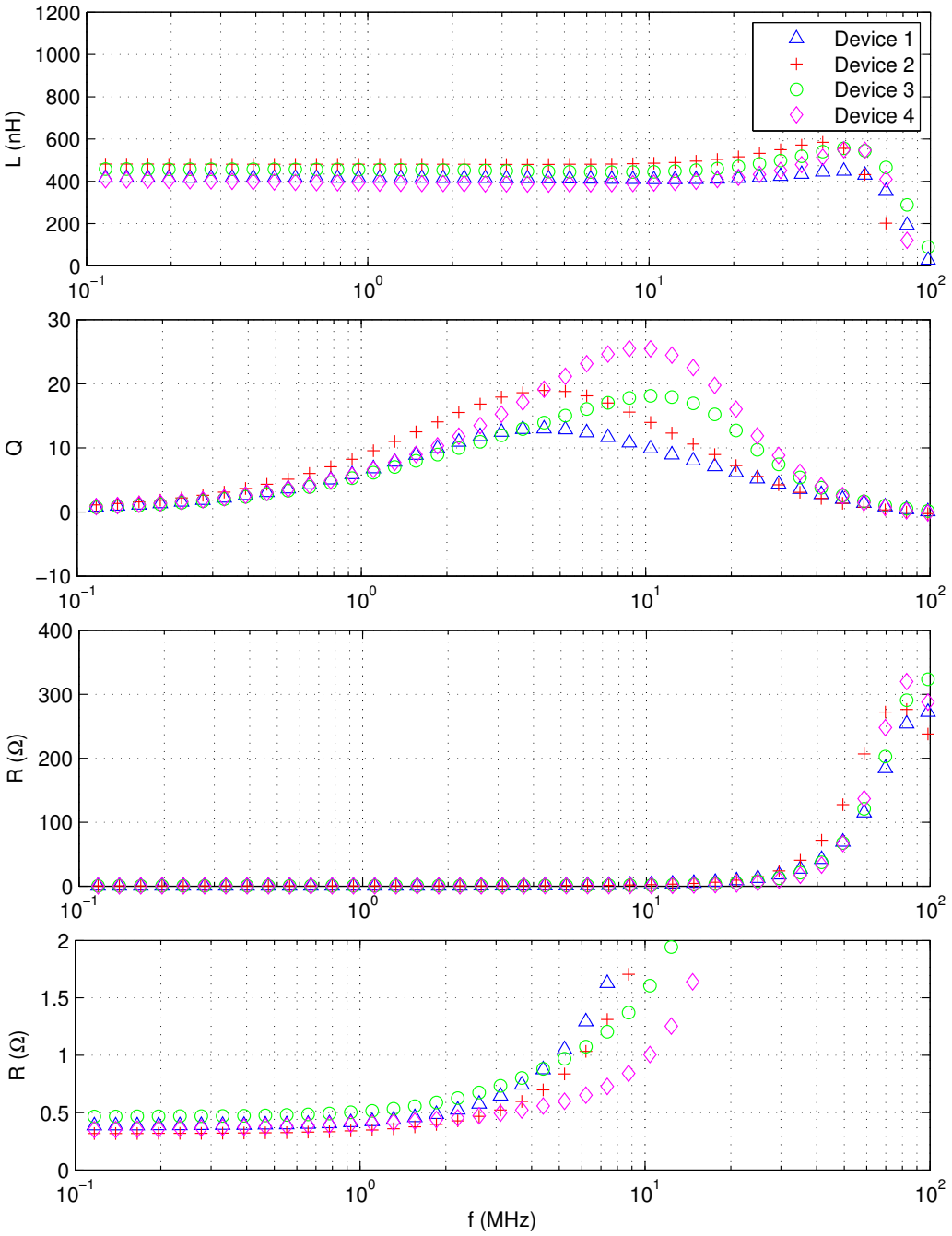


Figure 78: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with material mix -6 from Micrometals. Device 1-4 denote four inductors of nominally identical design as described in the text.

380-400 mm and an increased core thickness of 300-350 μm. As a result, inductances of 620-760 nH and quality factors of 37-38 around 10 MHz are achieved for devices

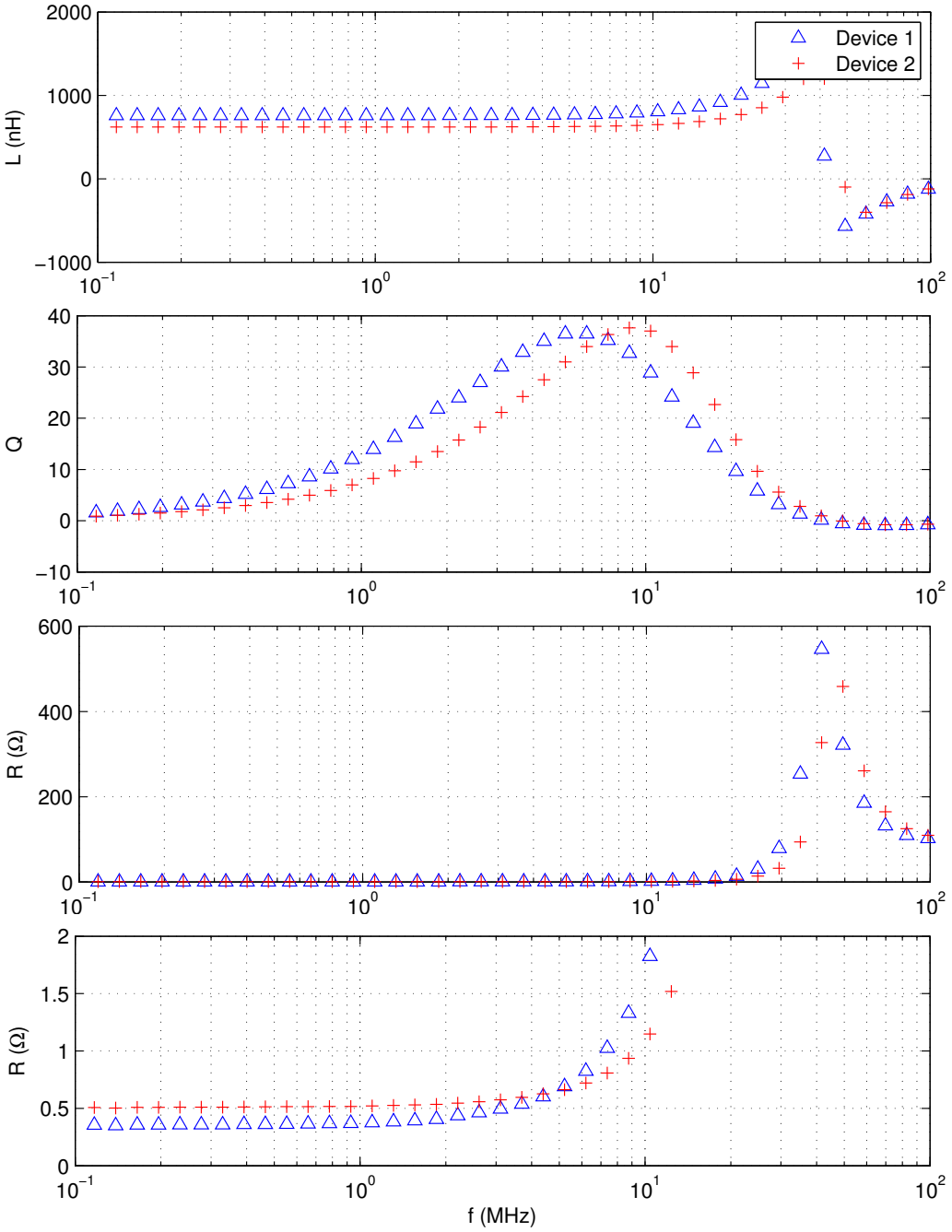


Figure 79: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with material mix -2 from Micrometals. Device 1 and 2 denote two inductors of nominally identical design as described in the text.

integrating material -2, while inductances of 407-482 nH and quality factors of 14-26 are achieved for devices integrating material -6, which also has a lower permeability

than material -2.

5.1.2.3 Ferrites

Ferrite materials generally exhibits a higher permeability than iron powder cores. They can be good alternatives when the inductance values provided by integrating iron powder cores are not sufficient. However, to avoid causing excessive losses in the embedded inductors, only ferrites with high resistivities, e.g. NiZn ferrites, are considered here.

Characterization results of the fabricated embedded inductors integrating ferrites from National Magnetics Group [76] and Fair-Rite [77] are shown in Figure 80 and 81 respectively. The properties of the integrated ferrites are shown in Table 5. Since the permeability of the ferrite materials is usually engineered for a targeted frequency range, appropriate materials should be selected for targeted applications based on their operating frequencies and loss tolerances. Generally, the higher the permeability, the lower the operating frequency of the inductor.

The fabricated inductors shown in Figure 80 have 24 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, and a copper thickness of 30 μm. The integrated cores have an inner diameter of 2.54 mm, an outer diameter of 5.08 mm and a thickness of 250-300 μm. Characterization shows inductances of 1.08 μH, 454 nH, and 143 nH and quality factors of 39, 42, 19 obtained for inductors integrating material M2, M3 and M5 respectively. As reference, the corresponding air-core inductor is also fabricated, which gives an inductance of 41 nH, as shown in the figure.

The inductor integrating material 67 in Figure 81 has the same geometry as those in Figure 80. Therefore given the core geometry shown in Table 5 for material 67, the inner edge of the core is trimmed using laser in order to be dropped into the embedded inductor. The inductor integrating material 68 has 50 turns, an inner diameter of 4

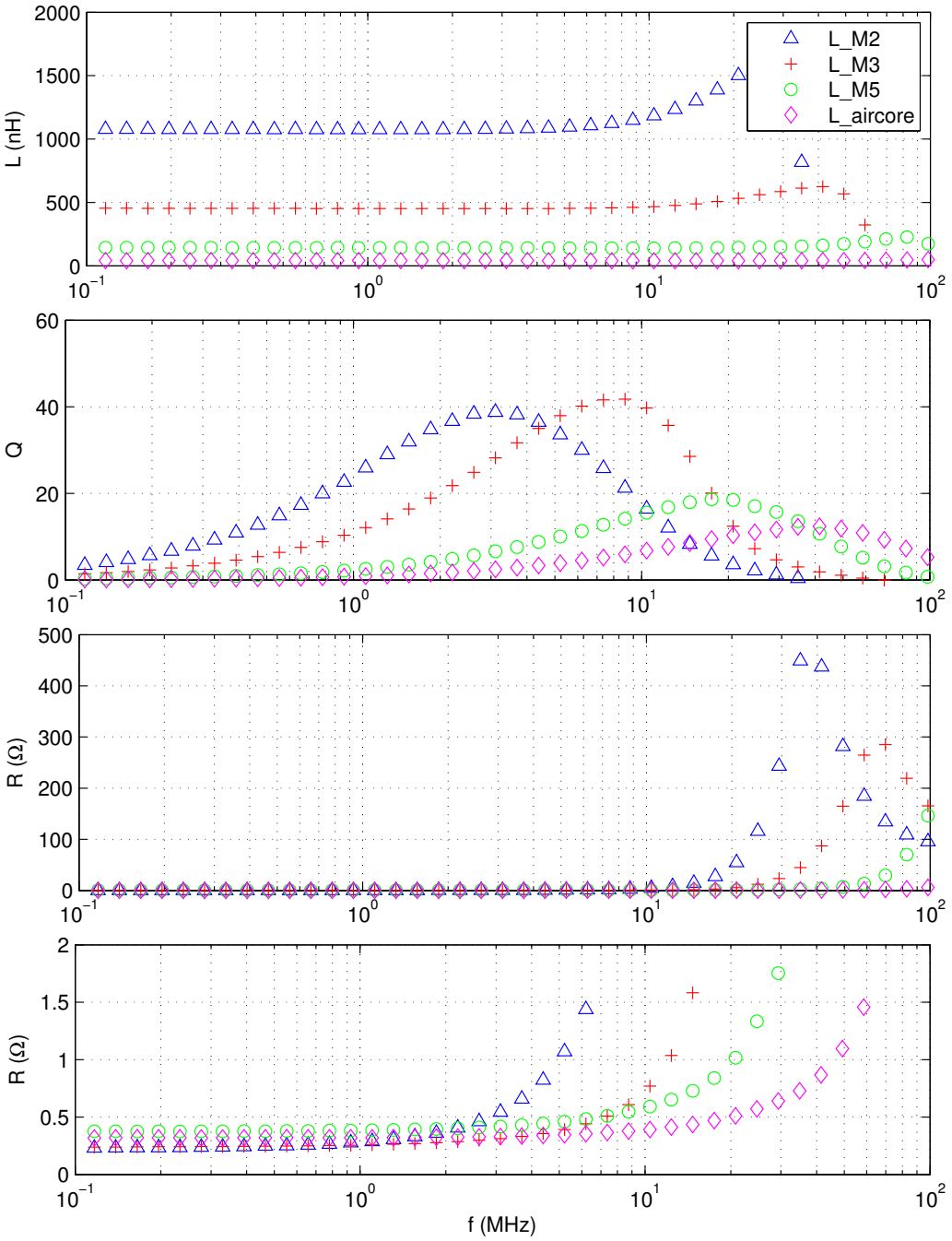


Figure 80: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with ferrite materials M2, M3, and M5 from National Magnetics Group.

mm, an outer diameter of 8 mm, a height of 300 μm, and a copper thickness of 30 μm. The outer edge of the core is trimmed using laser based on the core geometry in

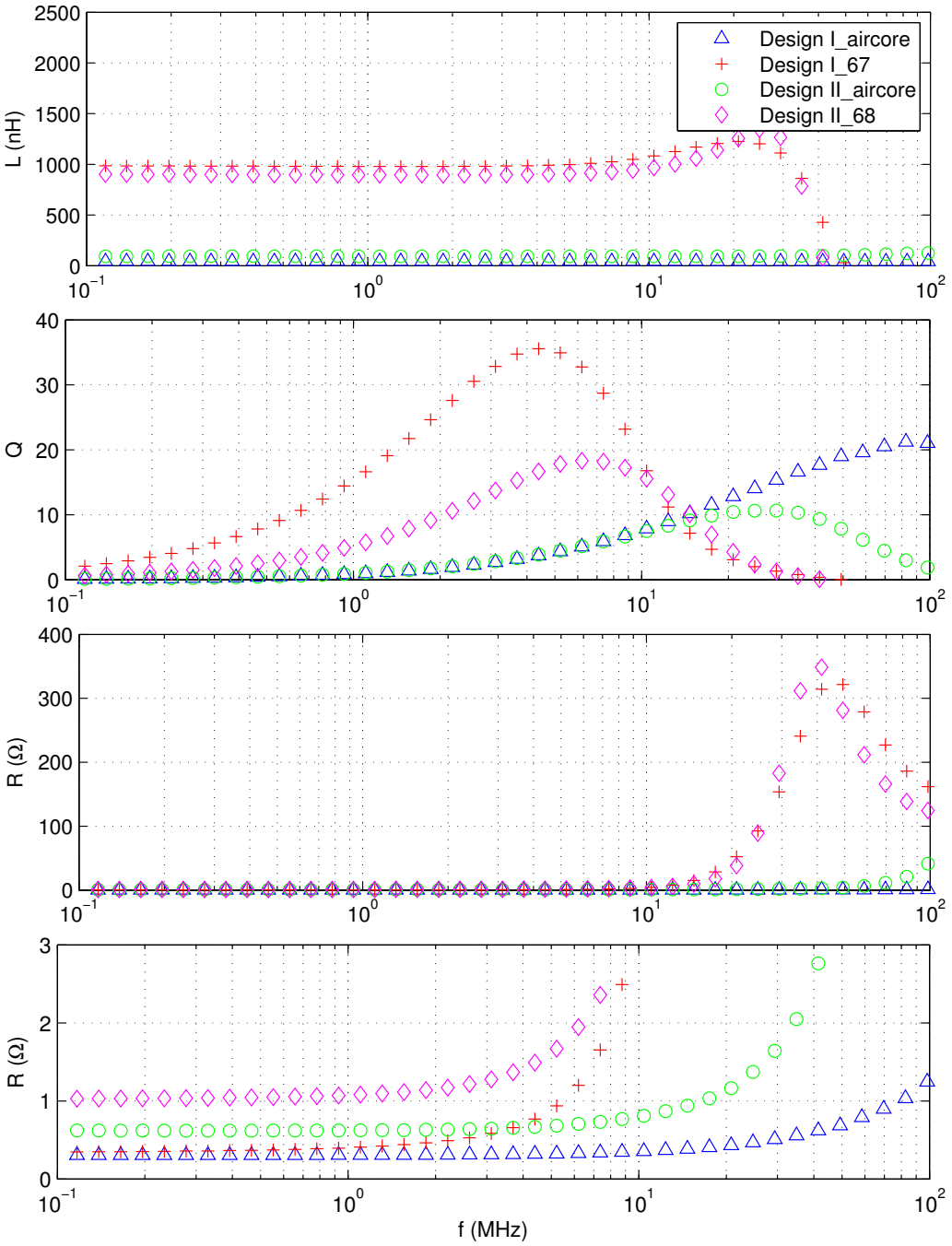


Figure 81: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with ferrite materials 67 and 68 from Fair-Rite.

order to be integrated into the embedded inductor. Inductances of 987 nH, 904 nH and quality factors of 35, 18 are achieved for inductors integrating material 67 and

Table 5: Properties of the Integrated Ferrite Cores

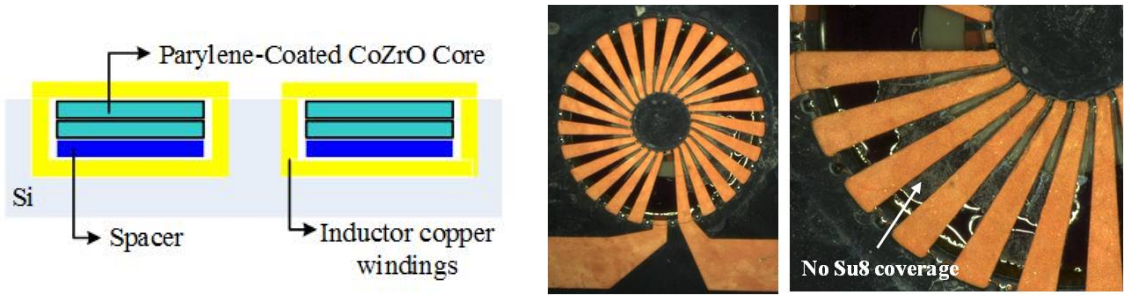
Ferrite material	Core Permeability	Core OD(mm)	Core ID(mm)
M2	40	5.08	2.54
M3	20	5.08	2.54
M5	7.5	5.08	2.54
67	40	5.95	2.95
68	16	9.7	4.6

68 respectively. The corresponding air-core inductors have an inductance of 43 nH and 93 nH respectively.

5.1.2.4 Metallic Cores

Besides commercial cores, academia-developed magnetic materials are also integrated into the embedded inductors using the fabrication technology we presented. Since the CoZrO material developed by Sullivan [78] exhibits a stable performance up to 100 MHz, it is chosen to be integrated into the embedded toroidal inductors. Using the deposition process developed in [78]–[82], CoZrO is sputtered onto both sides of a 50-μm-thick toroidal Alumina substrate with a total material thickness of 40 μm. The cores are then insulated with 5-μm-thick parylene and two of them are stacked inside the embedded inductor with a bottom spacer also inserted between the cores and the inductor bottom windings, as shown in Figure 82 (a). Images of the fabricated devices with CoZrO cores are shown in Figure 82 (b), with their characterization results shown in Figure 83.

The fabricated inductors have 24 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, and a copper thickness of 20-30 μm in standard-resistivity wafers. Two different bottom spacers are used in the integrated inductors: L1 has a 50-μm-thick bottom spacer of Alumina while L2 has a 25-μm-thick bottom spacer of polypropylene. An inductance of 290 nH and a quality factor of 33 at approximately 13 MHz is achieved for inductor L2. L1 demonstrates a much lower



(a) (b)

Figure 82: Schematic of CoZrO integration and the fabricated silicon-embedded inductors with CoZrO.

quality factor, which is probably due to the fact that the top conductors are closer to the CoZrO cores, therefore leading to more coupling losses in the metallic cores. The corresponding air-core inductor demonstrates an inductance of 41.8 and a quality factor of 8 at 11 MHz.

5.1.2.5 Summary

A summary of the characterization results for silicon-embedded inductors with both air core and integrated magnetic cores is shown in Figure 84 and Table 6. As labeled in the legend, LT stands for the lithography-based approach. SM stands for the shadow mask-based approach. HR stands for high resistivity. DL stands for double-layer winding inductors. Inductors 'Design I, LT' through 'Design I, DL' are air-core silicon-embedded inductors. IR stands for iron powder core and inductors 'Design I, IR-2' through 'CoZrO' are silicon-embedded inductors with various integrated magnetic cores.

From the results, we can see that embedded inductors with magnetic cores demonstrate significantly larger inductances and quality factors than air-core designs, including both ferrite materials and iron powder cores. Inductors with ferrites exhibit a better performance than inductors with iron powder cores since ferrites usually

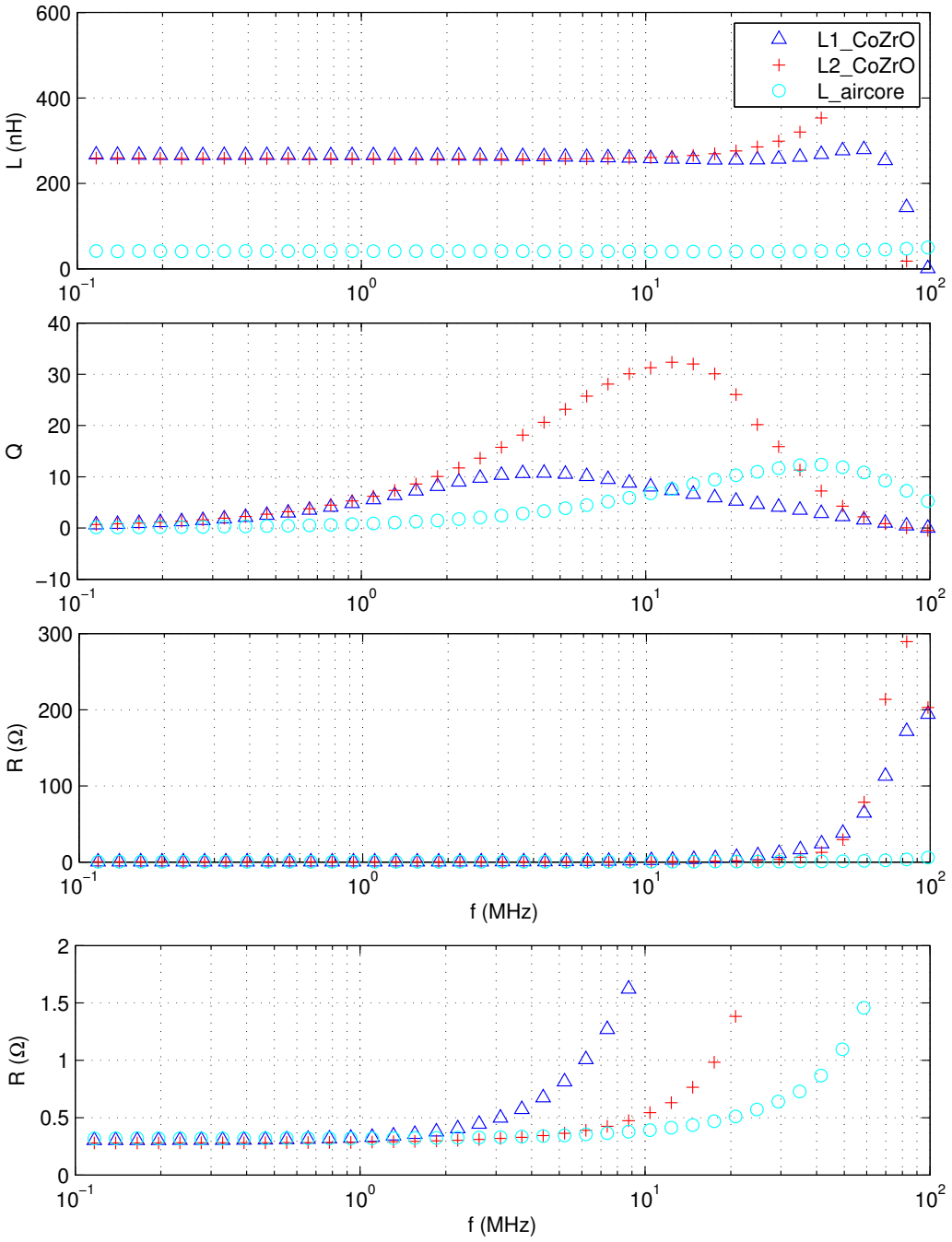


Figure 83: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the silicon-embedded inductors with metallic CoZrO cores(cite jizheng paper).

possess a larger permeability compared to iron powder cores. However, higher permeability is usually accompanied by a lower operating frequency. For our frequency

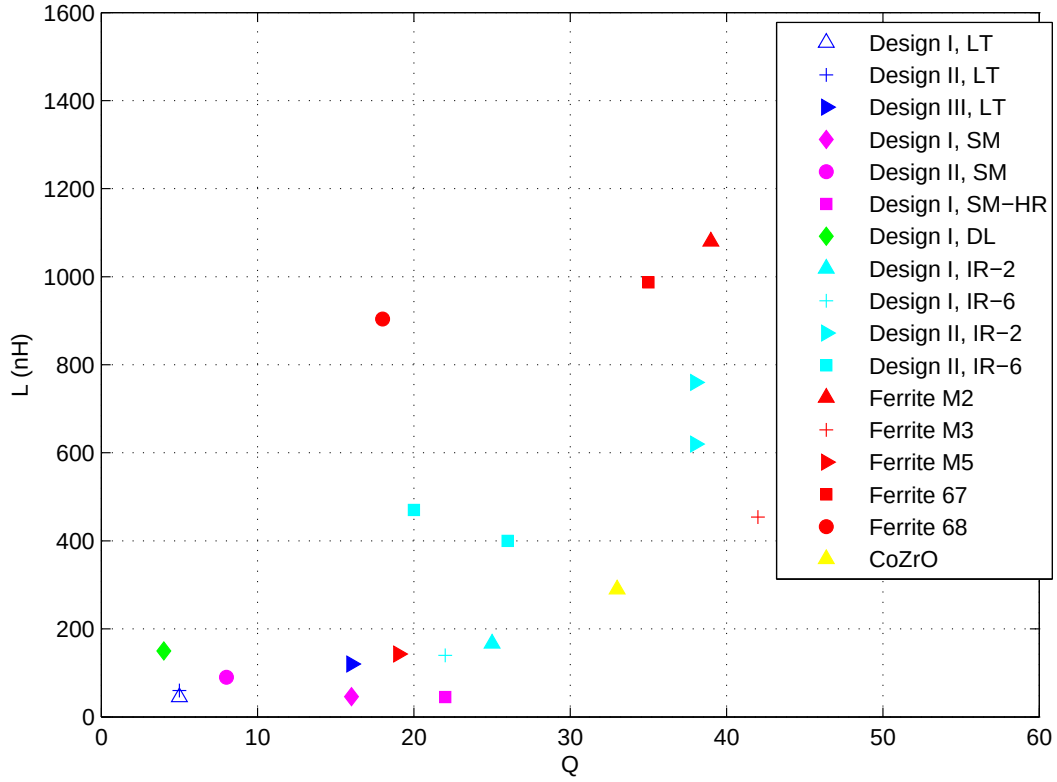


Figure 84: Summary of the fabricated silicon-embedded toridal inductors with both air core and magnetic cores.

of interest, iron powder cores (as suggested by performance of devices labeled as Design II, IR-2) are the best candidate for improving the performance of the silicon-embedded inductors because they could provide sufficient inductances and the peak quality factors occur within the frequency range of 5-30 MHz.

5.2 In-Circuit Testing

5.2.1 Large Signal Measurement Results

The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is largest at the maximum input voltage. Select an inductor with a saturation current higher than the maximum peak current and a break-down voltage larger than the

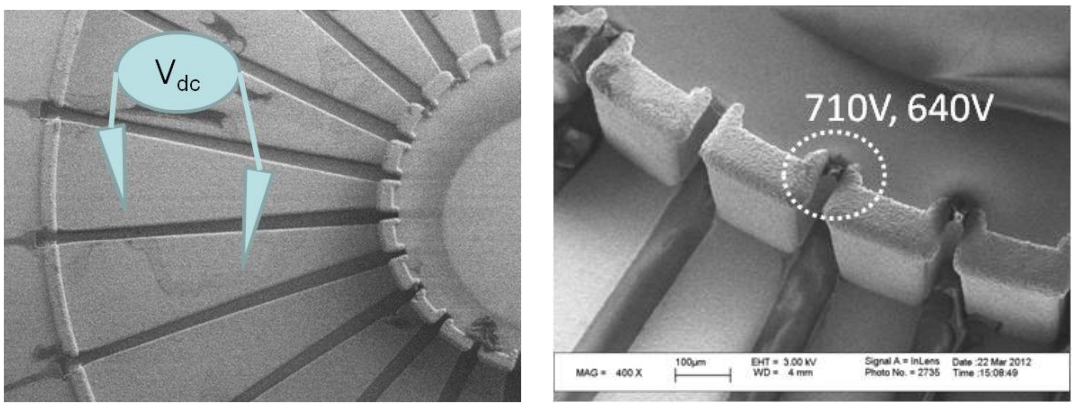
Table 6: Summary of Embedded Inductors with Both Air Core and Various Magnetic Cores

Core material	**Relative permeability**	**Inductance (nH)**	**Peak Q**
Design I, LT	1	45	5
Design II, LT	1	60	5
Design III, LT	1	120	16
Design I, SM	1	46	16
Design II, SM	1	90	8
Design I, SM-HR	1	45	22
Design I, DL	1	150	4
Iron Powder -2	10	760	38
Iron Powder -6	8.5	470	20
Ferrite M2	40	1080	39
Ferrite M3	20	454	42
Ferrite M5	7.5	143	19
Ferrite 67	40	987	35
Ferrite 68	16	904	18
CoZrO	20	260	32

input voltage is essential. Besides, heat dissipation capability of the inductor design should be examined to avoid device failure due to elevated temperature during continuous circuit operation.

The maximum DC current that could be passed through the inductor windings is determined by the thickness and width of the electroplated copper conductors as it is limited by the maximum current density allowable for copper. For the silicon-embedded inductors, the copper thickness is above 20 μm and a maximum DC current of 2A is able to be passed through the inductors.

The inductor break-down voltage is tested on devices fabricated with only bottom and vertical windings, as shown in Figure 85(a). There is a 12-μm-thick SiO_2 layer insulating the device from the silicon substrate, and the tested break-down voltage falls into the range of 640-740 V. The spots that a break-down usually happens are between adjacent vertical conductors where the distance between them is the closest, such as between the inner vertical conductors shown in Figure 85(b).



(a) (b)

Figure 85: Break-down voltage testing: (a) winding probing, and (b) break-down spots.

The temperature of the inductor operating in the circuit is approximately $100°C$. The material used in the silicon-embedded inductors can withstand the inductor operating temperature. Since the copper conductors in the silicon-embedded inductor are in direct contact with the silicon substrate, fast heat dissipation through silicon ensures that there is no overheating of the inductors with a fan during continuous operation mode of the power converter circuits.

5.2.2 Circuit Measurements

This section examines the performance of our targeted power converter circuit after employing the silicon-embedded toroidal inductors that we've fabricated. Photograph of the two-stage buck converter implemented on a printed circuit board (PCB) with the circuit topology presented before (developed by our collaborators in the ARPA-E program) is shown in Figure 86. The microfabricated inductors can be either flip-chip bonded, wire-bonded, or soldered with wires to connect to the PCB board of the power converter circuit, as shown in Figure 87.

The fabricated silicon-embedded inductors with iron powder cores, as characterized in Figure 78, are tested in the implemented circuit board and the results are

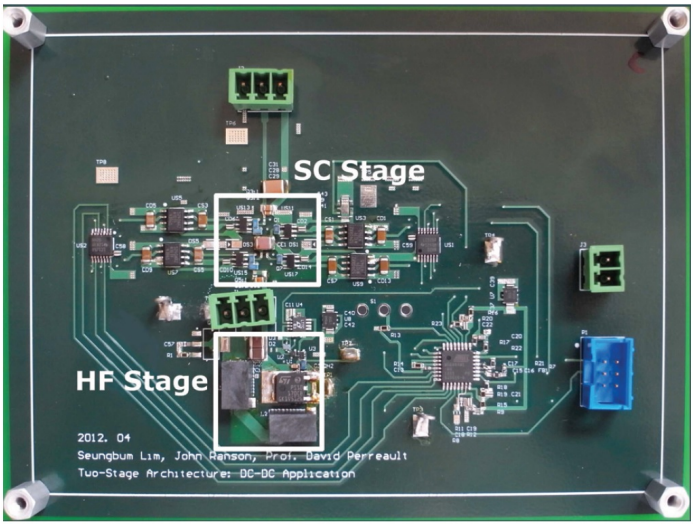


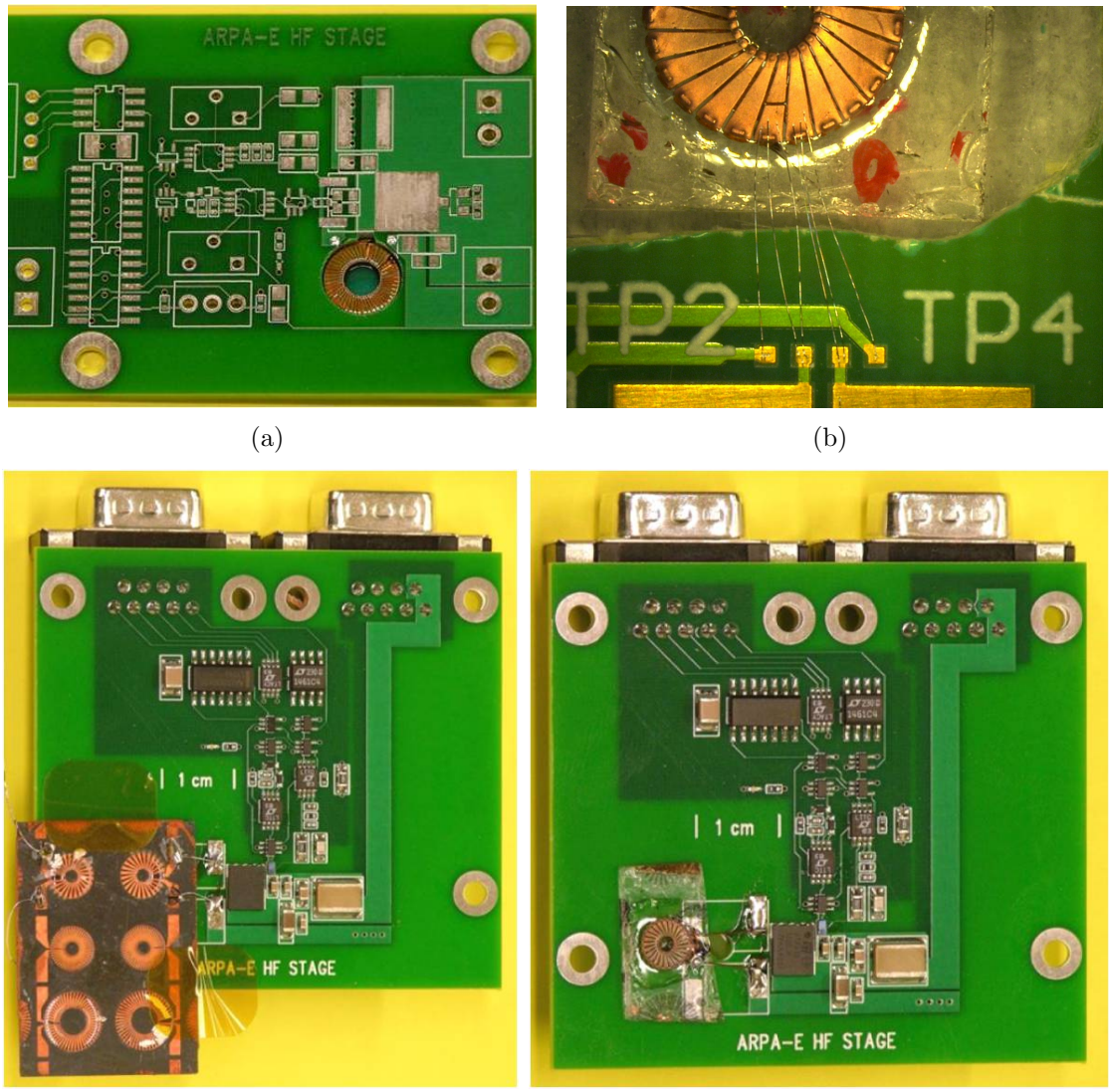
Figure 86: Photograph of the experimental prototype dc-dc converter with switched-capacitor stage and HF regulation stage outlined [15].

shown in Figure 88, 89 and 90.

Figure 88 presents the measured circuit efficiency at its corresponding switching frequency vs. circuit output power at a maximum input voltage of 100 V with the silicon-embedded inductors. L1 and L2 in the figure corresponds to Device 1 and 2 in Figure 78. A maximum efficiency of 91.13% is demonstrated at an output power of 40 W, a switching frequency of 7.8 MHz, and an input voltage of 100 V under pulsed operating conditions. Our designed circuit automatically adjusts switching frequency based on the inductance of the embedded inductor and the output power of the circuit. As can be seen from the figure, circuit efficiency increases with frequency decreasing as the output power increases.

Figure 89 shows the measured efficiency of the converter circuit at a wide range of input voltages using L1. As can be seen from the results, circuit efficiency increases with decreasing input voltages. At an input voltage of approximately 90 V, an efficiency of 92.33% is achieved at an output power of 40 W and a frequency of 7.8 MHz under pulsed operating conditions while the efficiency at an input voltage of approximately 50 V is 95%.

The measured waveforms of the real-time circuit operation are shown in Figure 90, including the real-time efficiency, real-time output power and real-time switching frequency. Since the output voltage is kept constant at 35 V, the output power waveform also stands for the output current waveform, which is also the current waveform in the silicon-embedded inductors.



(a) (b)

(c)

Figure 87: Photographs of converter circuit board integrated with microfabricated inductors using different methods: (a) flip-chop bonding, (b) wire-bonding, and (c) wire-soldering.

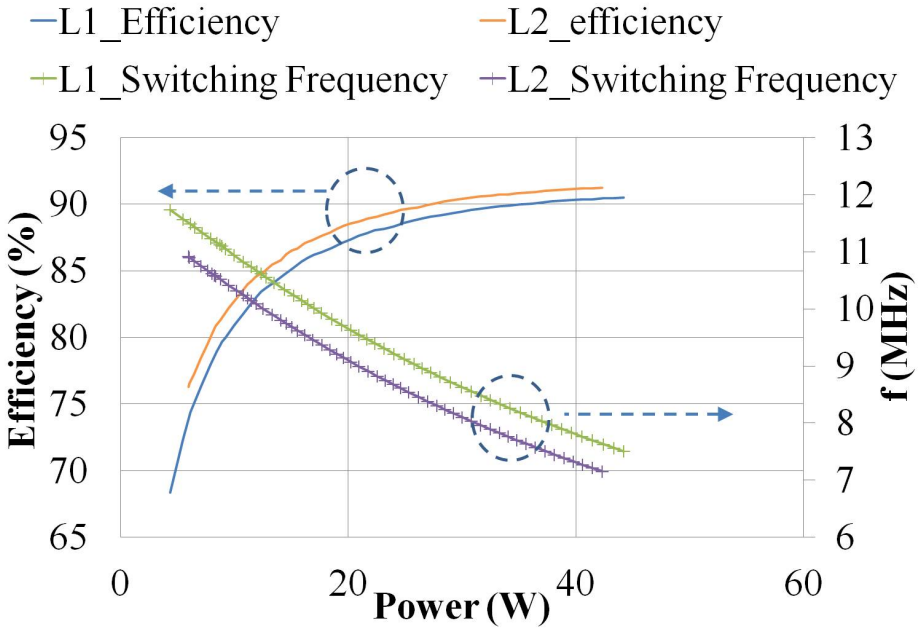


Figure 88: Measured efficiency at the corresponding switching frequency of the converter circuit operating at 100 V input voltage with silicon-embedded inductors integrating iron powder core (material -6).

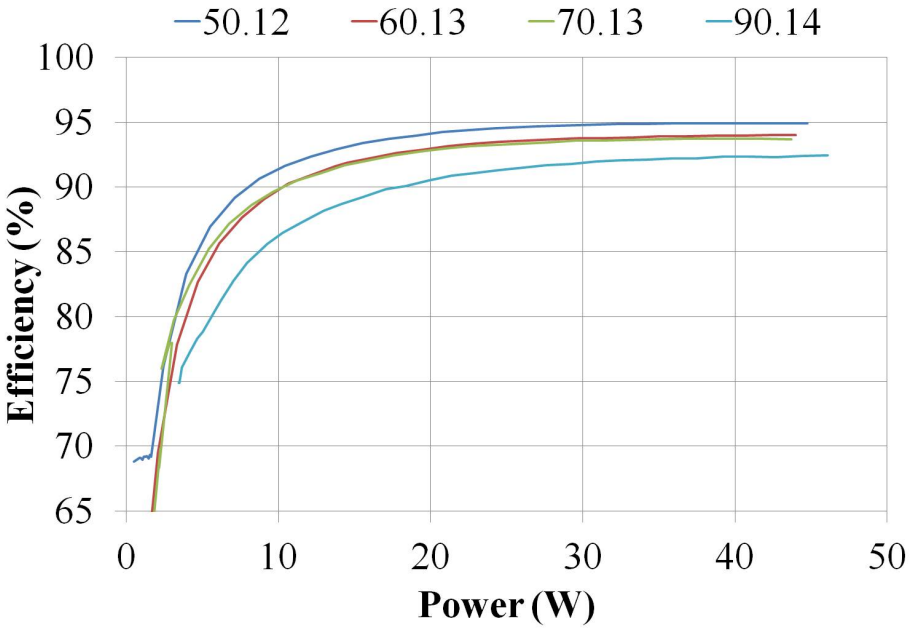


Figure 89: Measured efficiency of the converter circuit operating at a wide range of input voltages (50.12-90.14 V) with silicon-embedded inductors integrating iron powder core (material -6).

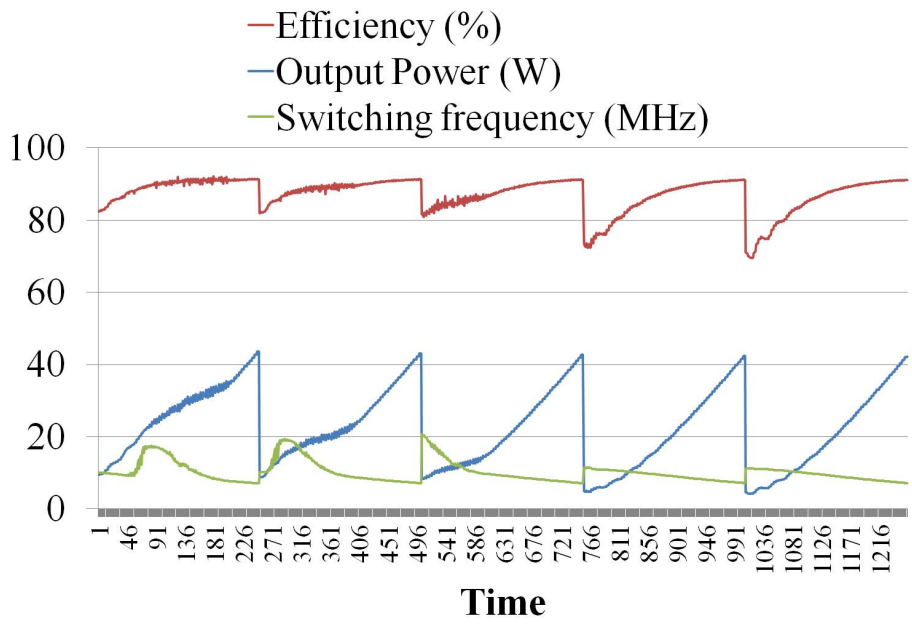


Figure 90: Measured waveform of the efficiency, output power and switching frequency in the circuit.

CHAPTER VI

OTHER APPLICATIONS OF EMBEDDED COMPONENTS

6.1 Transformer

Transformers comprise a critical part of many systems, such as electrical power distribution, portable power supplies and power converters, etc. They are used to raise or lower voltage and current between one circuit and another, and play a major role in almost all AC circuits. A transformer couples two circuits magnetically rather than through any direct connection, providing galvanic isolation and impedance matching when needed. Having integrated transformer devices that are embedded in silicon could provide a greater level of miniaturization for space-constrained systems.

Based on the double-layer winding technology that we developed, silicon-embedded transformers with a transformation ratio of 1:1 can be achieved using the same inductor fabrication process with only an alteration to the mask pattern for fabricating the top conductors. By arranging the connection of the top conductors to the vertical conductors in a slightly different way, as shown in Figure 91, two separate inductors that wrap around each other could be obtained. Having a single-layer top conductor geometry instead of two-layer top conductors simplifies the fabrication process of the embedded transformers as the latter would require deposition and patterning of an insulation layer in between the top conductors in addition to the two-layer conductor fabrication. Details of the fabrication process of the silicon-embedded transformers can be found in Figure 44.

Photographs of the fabricated silicon-embedded transformers with a turn ratio of 1:1 are shown in Figure 92. There are four pads on the device as shown in the figure,

two for testing the primary inductor and two for testing the secondary inductor. There are 24 turns in both the primary inductor and the secondary inductor. The transformer has an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm and a copper thickness of approximate 20 μm.

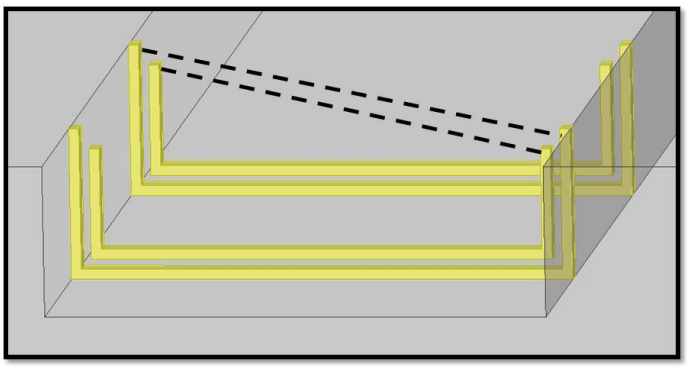


Figure 91: The winding connection scheme in silicon-embedded transformers.

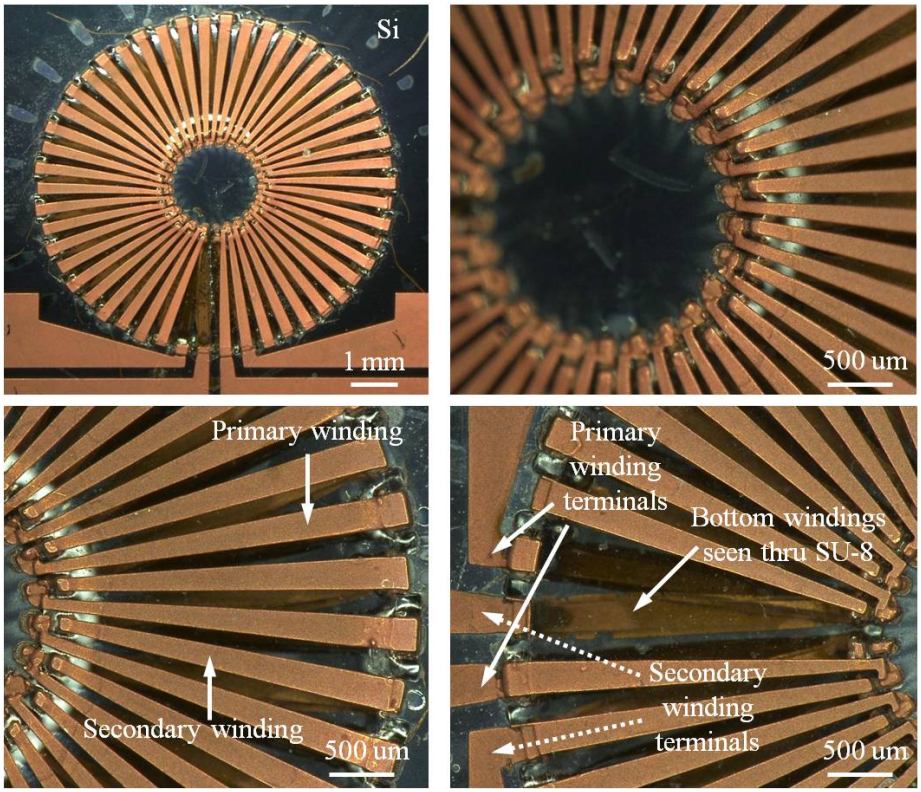


Figure 92: Fabricated silicon-embedded transformers based on the double-layer winding approach.

Characterization of the inductors on the primary and secondary side is first performed and the results are shown in Figure 93. Since the fabricated transformer has

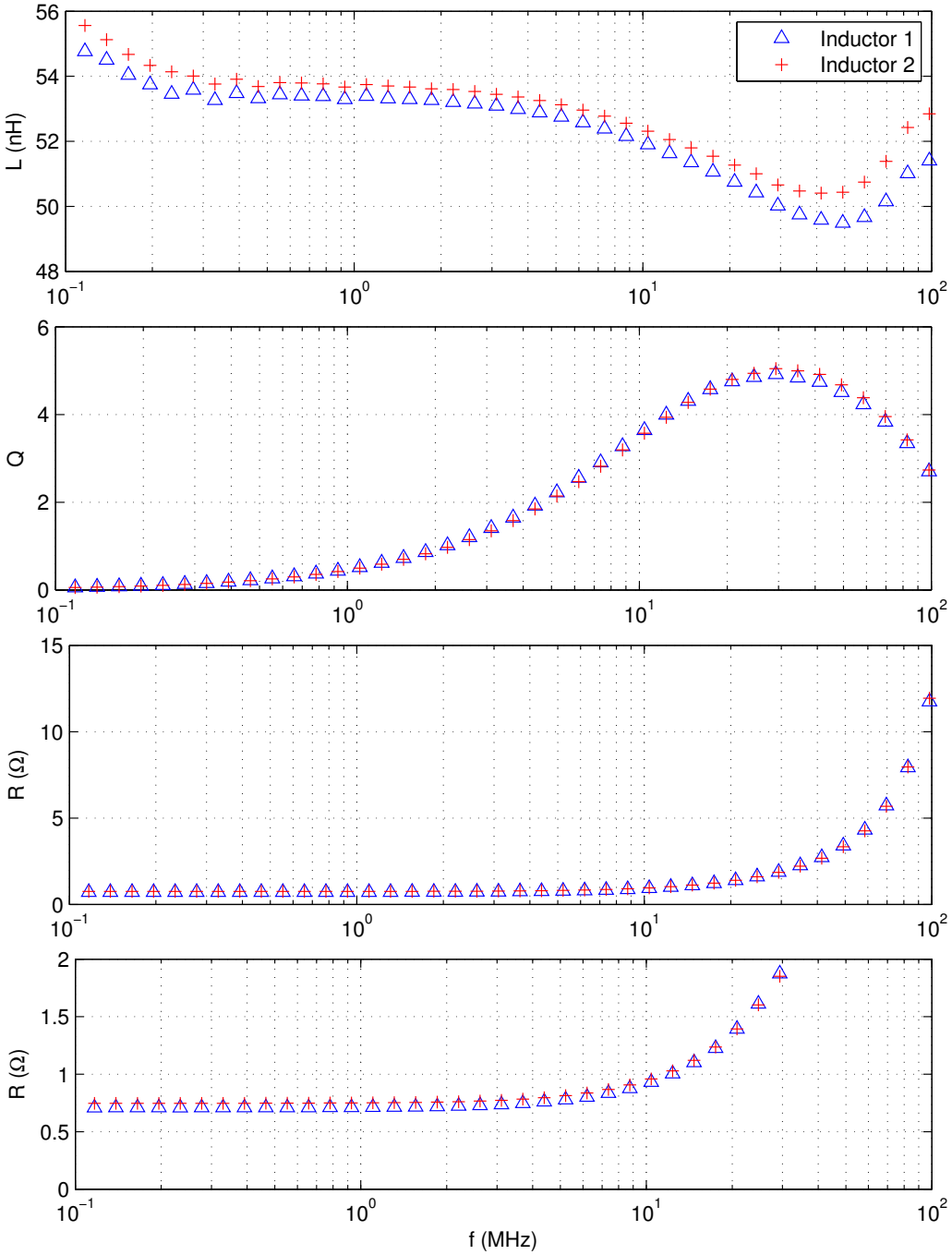


Figure 93: Measured inductance (L), quality factor (Q), and resistance (R) (complete view and magnified view) of the primary and secondary inductors in the silicon-embedded transformer.

a turn ratio of 1:1, the inductors on the primary and secondary side exhibit similar performances. An inductance of 55 nH and a quality factor of 5 is obtained for both inductors. The qualify factor of these inductors is lower than the embedded inductors fabricated with single-layer windings although they have similar geometries due to the fact that both the winding width and the copper thickness is reduced in the fabricated double-layer winding design, which therefore leads to an increased resistance of the inductor.

Different turn ratios can also be configured in the transformer by selectively fabricating a different number of windings on the inner layer than the outer layer. The maximum number of the windings on the inner layer cannot exceed the maximum number of the windings on the outer layer, however, since the inner-layer windings can serve as either the primary windings or the secondary windings, the embedded transformer can still be configured to be either a step-up or a step-down transformer in addition to the isolation transformer that we fabricated. Magnetic cores can also be integrated into the silicon-embedded transformers using the same drop-in approach that was developed for the embedded inductors to enable a better coupling between the primary inductor and the secondary inductor although it is not demonstrated here.

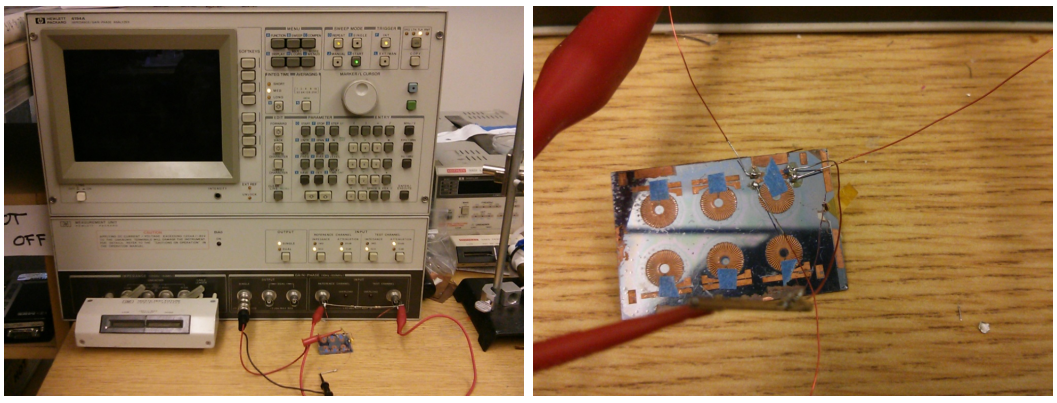
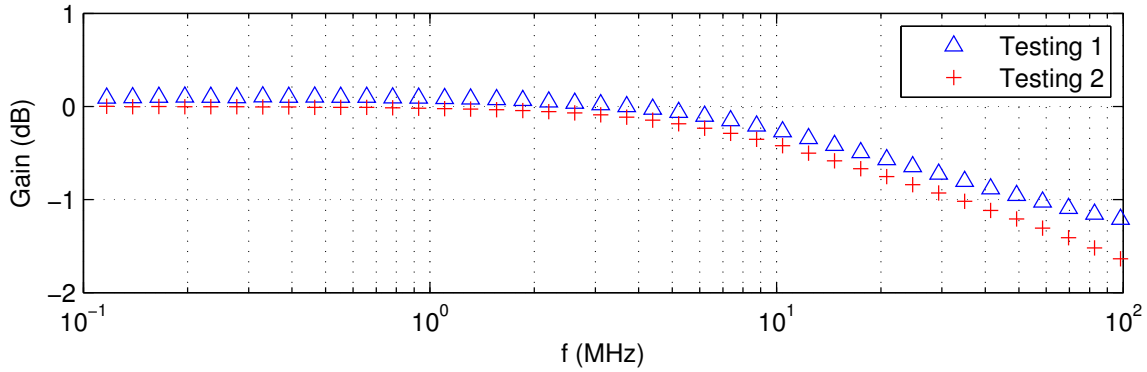
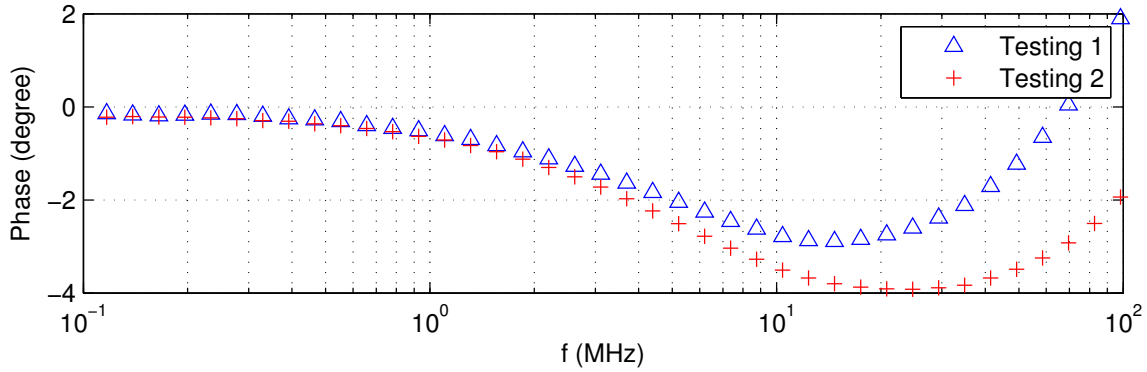


Figure 94: Experimental setup for characterizing gain-phase performance of the microfabricated silicon-embedded transformers.

The experimental setup for characterizing the gain and phase of the silicon-embedded transformers using an impedance analyzer (HP 4194) is shown in Figure 94 and the measurement results are shown in Figure 95-97. As a reference, transformers with wire-wound windings are also constructed and measured using the experimental setup. Photographs of the wire-wound transformers are shown in Figure 98, with integration of both a CoNiFe core and an iron powder core to improve the coupling between the primary and secondary windings. There are 9 turns in both the primary inductor and the secondary inductor using magnet wires (AWG 32), and from the measurement results in Figure 97 we can see clearly that these transformers demonstrate a gain of 0 dB and a phase of 180° for up to 10 MHz. However, with silicon-embedded transformers, different gain-phase behaviors are observed as



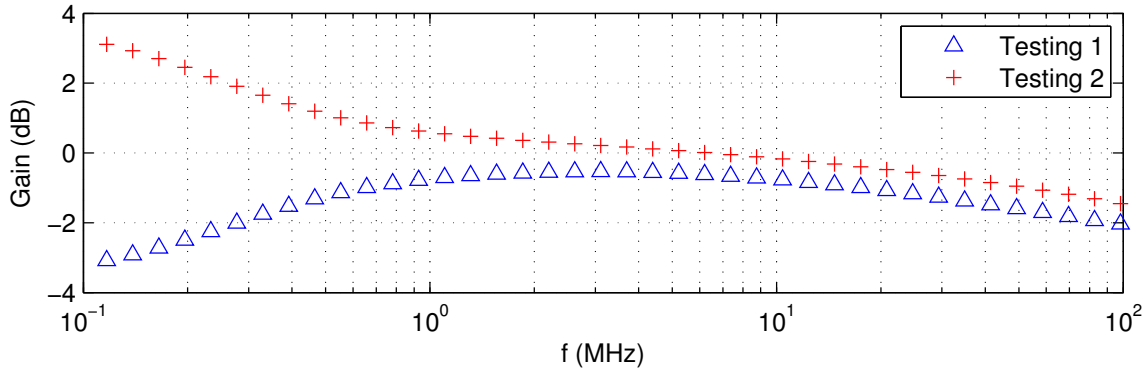
(a)



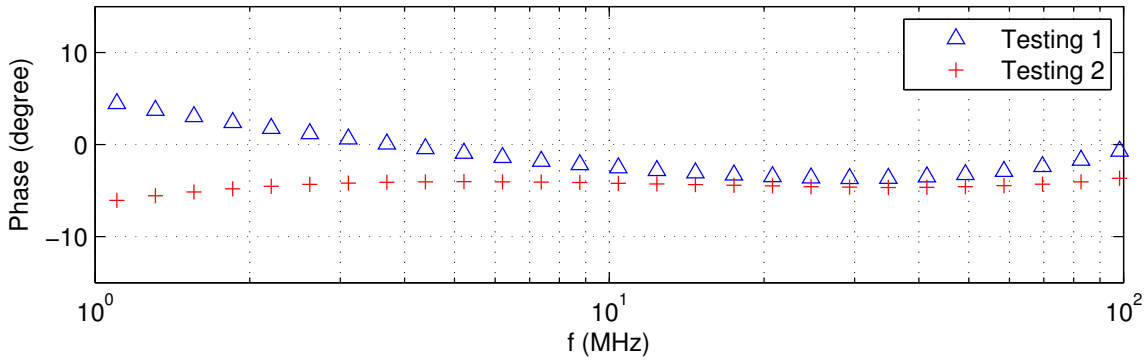
(b)

Figure 95: Gain-Phase measurement results of a silicon-embedded transformer.

shown in Figure 95-96, with each figure corresponding to an embedded transformer device under test. There are two sets of data in each figure (Testing 1 and Testing 2), which correspond to measurements of selecting one inductor as first the primary side and then the secondary side with the other inductor working first as the secondary side and then the primary side. A gain of zero and a phase of close to zero is measured in Figure 95 because the primary inductor and the secondary inductor in these transformers is shorted due to fabrication defects that originated from non-optimized processing steps. For example, misalignment in lithography steps can lead to shorted conductors, as shown in Figure 99(b), where one conductor belongs to the primary side and the other conductor belongs to the secondary side. There could also be shorts among windings on the same side, leading to a turn ratio other than



(a)



(b)

Figure 96: Gain-Phase measurement results of a silicon-embedded transformer.

1:1, which is the case in Figure 96. Consequently, the measured gain is not zero and switching the primary and secondary side leads to symmetrical responses. Although these devices are not demonstrated to function perfectly, these preliminary results still suggest that the fabrication process can be optimized to work properly and fully-functional silicon-embedded transformers can be expected to be a promising solution for realizing on-chip integration and miniaturization of many systems.

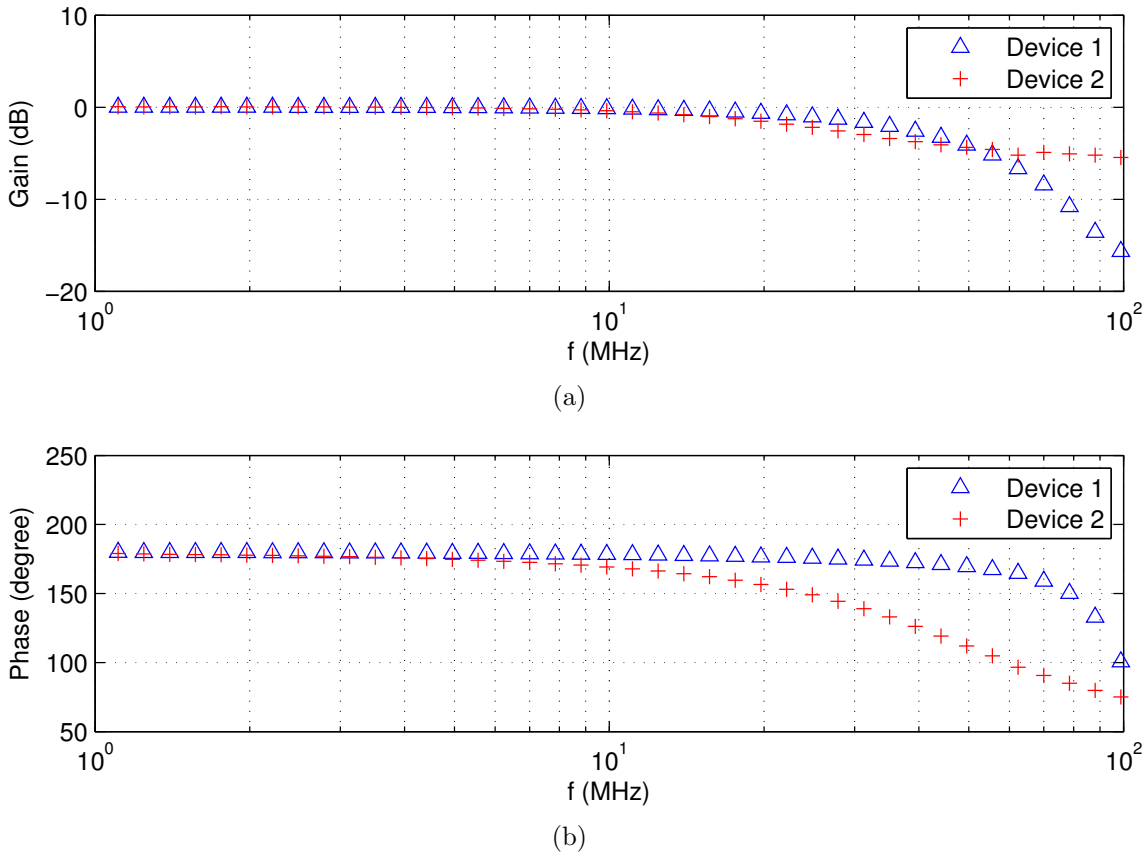


Figure 97: Gain-Phase measurement results of wire-wound transformers with CoNiFe(Device 1) and iron powder core (Device 2).

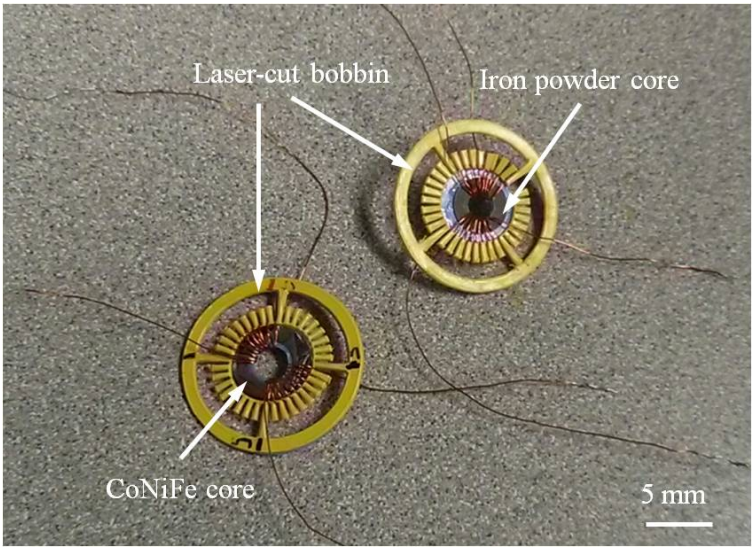
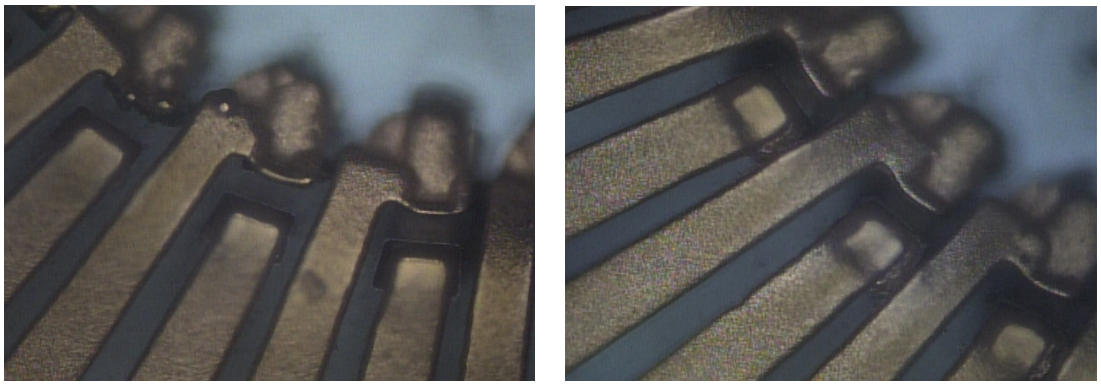


Figure 98: Photographs of the wire-wound transformers with both a CoNiFe core and an iron powder core.



(a) (b)

Figure 99: Fabricated windings with no misalignment (a) and (b) misalignment that causes shorts between primary and secondary windings.

6.2 Wireless Power Transfer

Recently, wireless power transfer has gained significant interest as a technology to realize contactless battery charging [83], [84]. Successful powering of implantable microsystems [85], cell phones [86] and desktop peripheral applications [87] has been demonstrated where the application device was equipped with receiver coils and wirelessly charged when being coupled closely to the transmitter coils. Commercial

products have also been developed [88] and having cable-free homes with all devices charged wirelessly is believed to be the future.

The mechanism behind wireless power transfer is that, the current in the transmitter coils generates an alternating electromagnetic field, which then interacts with the receiver coils to generate a current or voltage-drop in it. When transmitter and receiver coils are designed to resonate at the same frequency, resonance-based energy transfer [86] occurs and enables efficient power transfer over large distances. Due to its resonance nature, energy will be coupled mostly to objects of the same resonant frequency and less to off-resonant objects. Further, when high quality-factor coils are employed as the transmitters and receivers, resistive losses in the circuits are reduced and efficient mid-range power transfer can therefore be achieved. In contrast to the close-range power transfer using non-resonant inductive-coupling mechanism, mid-range wireless power transfer is typically implemented over distances ranging from two to ten times the coil size.

For applications requiring multi-watt power levels using mid-range wireless power transfer, such as handhold electronics and home appliances, developing a low-profile receiver coil with a high energy transfer efficiency is the challenge. Having a silicon-embedded receiver coil that is integrated with circuits on a single silicon chip could provide an enormous level of miniaturization of the whole system. In this chapter, our preliminary efforts in developing first a Kapton-based planar receiver coil and then a low-profile solenoid receiver coil with reasonable transfer efficiencies will be presented. The paragraphs proceed first with understanding the circuit theory behind the power transfer and then a demonstration of both an air-core planar receiver coil and a magnetic-core solenoid receiver coil for wireless power transfer.

6.2.1 Power Transfer Circuit Analysis

A simplified schematic of a typical setup for wireless power transfer is shown in Figure 100, where V_s represents an ideal power source, R_L is the load resistance to which power will be wirelessly transferred, M is the mutual inductance between the coupled transmitter and receiver coil inductors L_1 and L_2, C_1 and C_2 are the capacitances used to set the circuit resonant frequency (with $\frac{1}{L_1C_1} = \omega_0^2$ and $\frac{1}{L_2C_2} = \omega_0^2$), and R_1, R_2 are resistances of the inductors.

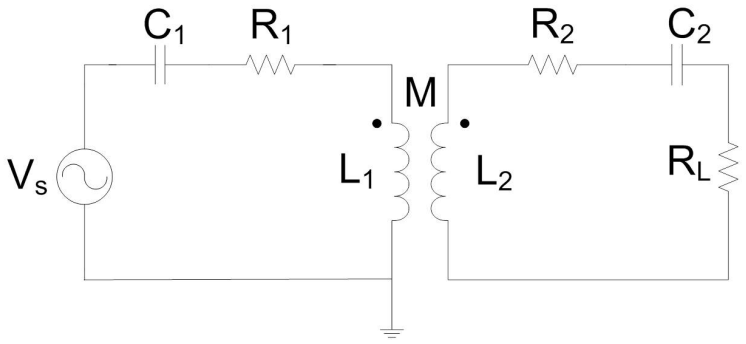


Figure 100: Simplified schematic of a typical setup for wireless power transfer.

The power transfer efficiency at resonance, η, is defined as the power absorbed by the load divided by the total input power extracted from the power source, which is formulated as [89] based on the circuit in Figure 100:

$$\eta = \frac{\omega_0^2 M^2 R_L}{(R_2 + R_L)^2 Z_1}, \tag{10}$$

$$Z_1 = R_1 + \frac{\omega_0^2 M^2}{(R_2 + R_L)}, \tag{11}$$

where ω_0 is the circuit resonant frequency and Z_1 is the impedance seen by the power source V_s that incorporates the effect of the load resistance when the receiver coil is coupled to the transmitter coil. To gain a better insight into the circuit, equation (10) is combined with equation (11) and rearranged as:

$$\eta = \frac{R_L}{R_2 + R_L} \cdot \frac{\omega_0^2 M^2}{R_1(R_2 + R_L) + \omega_0^2 M^2}. \tag{12}$$

In the case of an ideal transmitter coil that has no resistive loss and is coupled only to the receiver coil, that is, $R_1 = 0$ and $Q_1 = \infty$, the transfer efficiency, denoted as η_∞, reduces to

$$\eta_\infty = \frac{R_L}{R_2 + R_L}, \tag{13}$$

which depends only on the receiver circuits. If the receiver coil also has zero resistance and infinite Q_2 as in an ideal case, the transfer efficiency becomes independent of the mutual inductance and the load (this unrealistic case is due to the assumptions of ideal drive source and zero parasitics; although no real power is lost, significant reactive power will be present in the circuits). In reality, resistive loss is present in the inductor and its quality factor is a finite value. In such a case, the transfer efficiency can be represented as an ideal efficiency for the case of an ideal transmitter coil, η_∞, times an attenuation factor determined by the quality factors and the coupling effect:

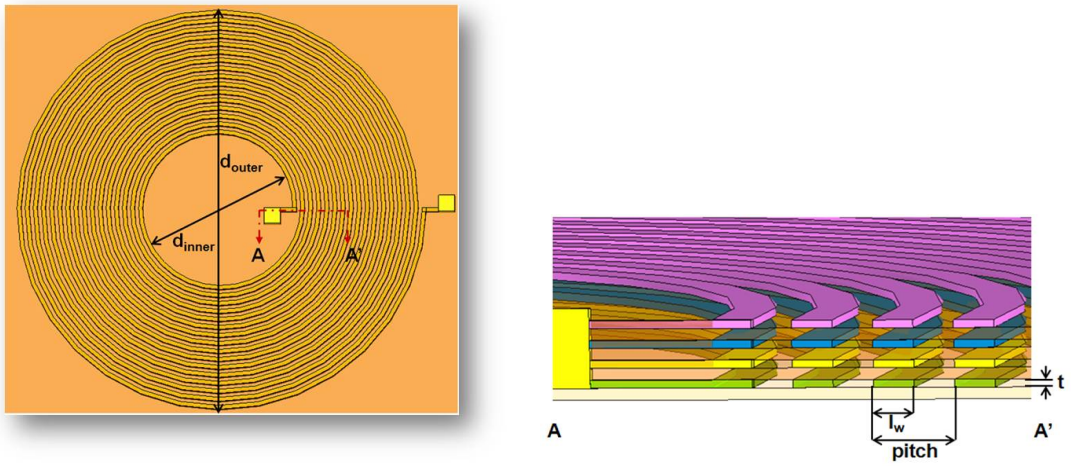
$$\eta = \eta_\infty \cdot \frac{1}{1 + \frac{1}{k^2 Q_1 \cdot Q_{2,l}}}, \tag{14}$$

where k is the coupling coefficient with $M = k\sqrt{L_1 L_2}$, Q_1 is the unloaded quality factor of the transmitter coil with $Q_1 = \frac{\omega_0 L_1}{R_1}$, and $Q_{2,l}$ is the loaded quality factor of the receiver coil, defined as $Q_{2,l} = \frac{\omega_0 L_2}{R_2 + R_L}$.

Clearly, for a given load, the key factors for enabling a high power transfer efficiency are a high unloaded quality factor of the transmitter coil, a high loaded quality factor of the receiver coil, and a high coupling coefficient between them. Since the transmitter coil is usually designed to be large and have high quality factors, the key is to have low-profile receiver coils that satisfy the performance requirements.

6.2.2 Planar Receiver Coil

As an initial effort, an air-core spiral inductor implemented using flexible PCB technology is explored as the receiver coil. The planar inductor is designed with multiple vertical laminations and varying turn widths to maximize the quality factor, as shown



(a) (b)

Figure 101: Schematic of the multi-layer spiral inductor, (a) top view, and (b) partial cross-sectional view.

in Figure 101. Axisymmetric two-dimensional (2-D) electromagnetic simulations are performed to verify the design. The use of flexible printed-circuit-board (PCB) fabrication techniques potentially enables not only relatively low-cost manufacturing, but also conformable and space-efficient incorporation of coils into more complicated systems. Experiments measuring inductor performance as well as demonstrating wireless power transfer are conducted, and results are presented. Although the operating frequency is fixed to 300 kHz in this work, the method presented is applicable to other frequencies.

6.2.2.1 Planar Inductor Design and Simulation

As discussed above, one of the key factors for enabling efficient resonant power transfer is the high quality factor of the receiver coil, given that the transmitter and receiver coils have been tuned to operate at the same resonant frequency. The quality factor of a spiral inductor can be calculated from its inductance and resistance at a given frequency:

$$Q = \frac{\omega L}{R_\omega}, \tag{15}$$

where ω is the angular frequency, L is the inductance, and R_ω is the overall resistance of the inductor at the resonant frequency.

The inductance at low frequency in the absence of permeable material can be approximated well using the formula [90]:

$$L_s = \frac{\mu_0 n^2 d_{avg}}{2}(\ln \frac{2.46}{\rho_s} + 0.2\rho_s^2), \tag{16}$$

$$d_{avg} = \frac{d_{outer} + d_{inner}}{2}, \tag{17}$$

$$\rho_s = \frac{d_{outer} - d_{inner}}{d_{outer} + d_{inner}}, \tag{18}$$

where μ_0 is the permeability of free space, n is the number of total turns in the inductor, d_{avg} is the average diameter of the inductor, d_{outer} is the diameter of the outermost turn, d_{inner} is the diameter of the innermost turn and ρ_s is a geometrical fill ratio as defined.

Since practical circuit considerations limit the voltage levels in the coils, these voltage limits translate into a limit on the coil inductance values in our system on the order of tens of microhenries. Further, the dimensions of the windings can be chosen to be on the order of twice the skin depth as a rule of thumb, resulting in the pitch between turns, as defined in Figure 101, to be on the order of hundreds of micrometers. The outer diameter of the inductor is fixed due to the footprint requirement of our application. Once these parameters have been chosen, equation (16) can be used to determine the total number of turns.

The resistance of the planar inductor includes DC resistance and AC resistance:

$$R_w = R_{dc} + R_{ac} = R_{dc}(1 + \alpha_{ac}). \tag{19}$$

By approximating all spiral windings to be concentric circles, DC resistance can be formulated as:

$$R_{dc} = \frac{\rho l}{l_w t}, \tag{20}$$

$$l = \frac{\pi n(d_{outer} + d_{inner})}{2}, \tag{21}$$

$$d_{inner} = d_{outer} - 2n(l_w + l_g), \tag{22}$$

where ρ is the resistivity of copper, l is the total length of all the turns in the inductor, l_w is the width of a single turn, l_g is the gap between adjacent turns, and t is the thickness of the copper.

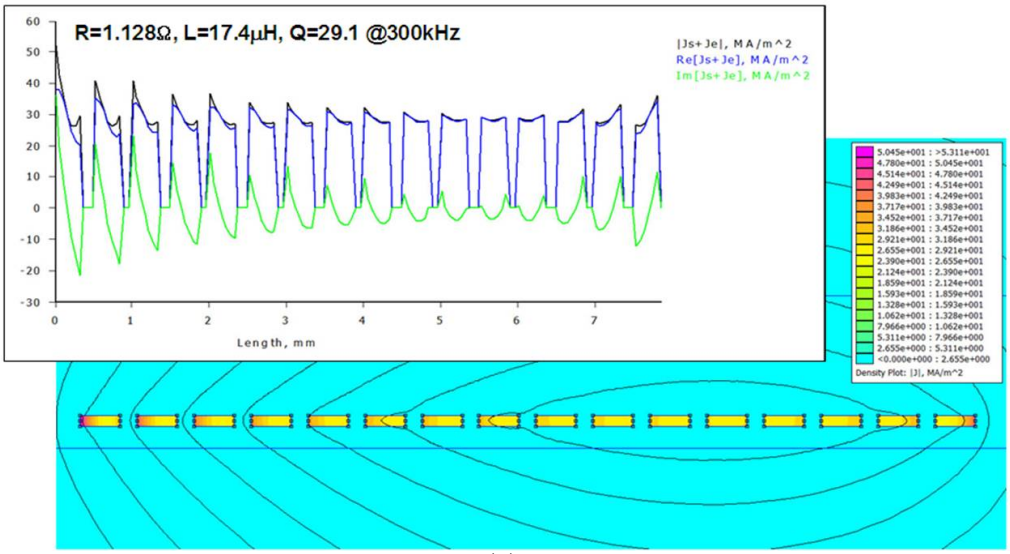
The AC resistance models the skin depth effect and proximity effect in the turns at high frequencies, and a coefficient α_{ac} is used to denote the dependency of the AC resistance on parameters such as frequency, skin depth, copper thickness, turn number, turn width and turn pitch [91]–[93].

For a given inductance, by substituting equations (19, 20, 21, 22) into equation (15), the quality factor becomes:

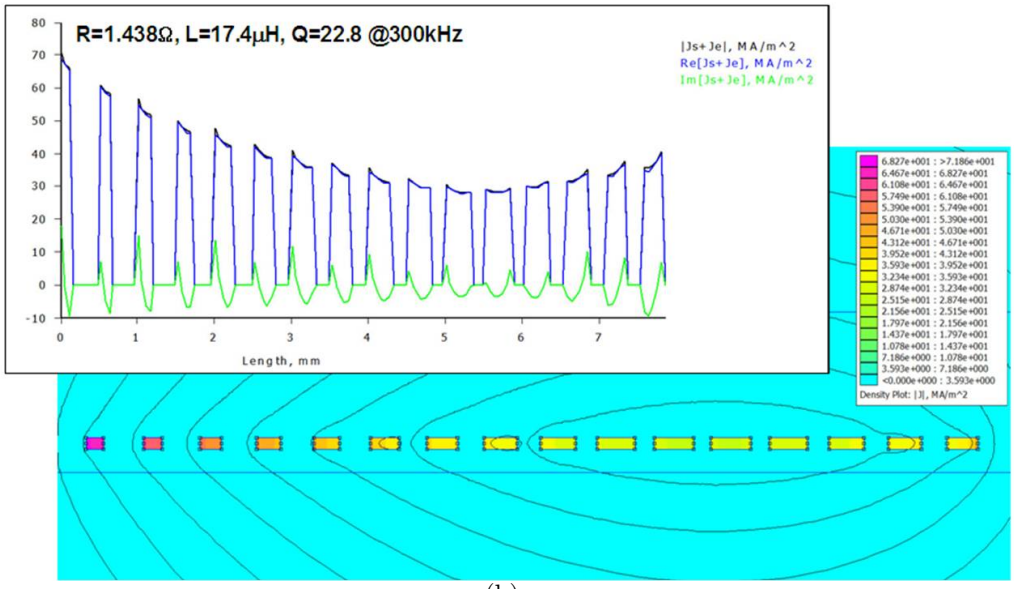
$$Q = \frac{1}{1 + \alpha_{ac}} \cdot \frac{\omega L}{\pi \rho} \cdot l_w \cdot t \cdot \frac{1}{n[d_{outer} - n(l_w + l_g)]}. \tag{23}$$

The effect of the DC resistance on the quality factor will first be discussed analytically, followed by simulations to determine the effect of the AC resistance on the quality factor (i.e., the magnitude of the expression $\frac{1}{1+\alpha_{ac}}$).

Since the inductance value and the outer diameter of the coil are fixed, the pitch between turns determines the total number of turns. Therefore, for a given pitch, the turn number is fixed and what remains in equation (23) is only the turn width and winding thickness. Because of the linear relationship between quality factor and the turn width, a maximized quality factor can be obtained with a maximized turn width, which is, however, practically limited by how small the gap could be realized through fabrication processes. Similar constraints exist for the winding thickness. Although the thicker the copper, the higher the Q-factor, fabrication technology constrains the maximum thickness that can be achieved. So in conclusion, with a maximized copper thickness and a minimized turn spacing within fabrication capability, an optimized quality factor of a single-layer planar inductor can be achieved by finding the



(a)



(b)

Figure 102: Current density distribution for a single-layer 16-turn inductor with (a) uniform turn width of 350 μm and (b) variable turn width ranging from 150 μm to 350 μm. Both have a constant turn pitch of 500 μm.

optimized combination of turn-to-turn pitch and turn number.

However, with a single-layer design in a limited footprint, the improvement in quality factor available from varying the pitch and turn number is still limited. To address this issue, a vertical lamination concept is proposed to overcome the area

constraint to further increase the quality factor. In addition, we also introduced a concept of varying-width design to further improve the inductor performance, as shown in Figure 102. To achieve the vertical lamination, optimized single-layer inductors with varying turn widths are stacked together and separated by thin layers of Kapton film. The multiple inductor layers are then connected in parallel to reduce the resistance of the overall inductor. Due to the almost perfect coupling between adjacent layers, the overall inductance of the laminated inductor remains the same as a single-layer inductor since the added mutual inductance between layers compensates for the reduction in inductance resulting from a parallel-connected configuration.

2-D electromagnetic simulations using the simulation package FEMM were conducted to determine the optimized current density distribution inside the turns for varying width designs. Figure 102 shows a comparison between the original design with uniform turn width and a design with varying turn width. The inductor with uniform width design does not have uniform current distribution throughout the cross-section of each turn. For example, the 5th turn from inner end have the most uniform current distribution while the turns farthest from it suffer from severe proximity effect, which creates the large current peaks near the boundaries of the windings. To suppress this eddy current loss, the width of each turn is modified as shown in the figure. Starting from the position of minimum proximity effect and going to the inner and outer edge of the coil, the width of each turn is reduced gradually by 20 μm while the pitch between turns is fixed. A better uniformity in the current density distribution is achieved with no obvious current peaks near the boundaries. The high current density value is due to the reduced cross-section of the windings. Although the quality factor of a single layer inductor with variable width is typically lower than that of a constant width design, as will be seen later, this effect is reversed for stacked layers.

Table 7: Simulated Q-factor, resistance and inductance values for varying width inductors with different turn widths and spacings. The width and spacing values are the original values before applying variable width design.

	Gap [μm]		
Width [μm]	50	100	150
250			Q = 67.8 Rdc = 0.461 Ω R300 = 0.530 Ω L = 19.1 μH
300	Q = 72.2 Rdc = 0.415 Ω R300 = 0.524 Ω L = 20.1 μH	Q = 71.9 Rdc = 0.406 Ω R300 = 0.493 Ω L = 18.8 μH	Q = 70.4 Rdc = 0.401 Ω R300 = 0.590 Ω L = 17.7 μH
350	Q = 73.9 Rdc = 0.367 Ω R300 = 0.477 Ω L = 18.7 μH		Q = 72.8 Rdc = 0.353 Ω R300 = 0.428 Ω L = 16.6 μH

An optimized design was then found through finite element simulations for different combinations of turn width and gap values using varying width design, as shown in Table 7. The simulated inductor has a four-layer lamination with a vertical inter-layer gap of 125 μm, and each layer has an outer diameter of 5 cm, a copper thickness of 100 μm, and a turn number of 16. The turn width varies from 250 μm to 350 μm, as shown in the table 7, and the gap between turns varies from 50 μm to 150 μm. For a constant pitch, such as the designs along the diagonal line from upper right to bottom left, the quality factor increases with an increasing width and shrinking gap, which agrees well with the analytical result. The maximum quality factor is obtained with a combination of 350 μm width and 50 μm gap, which is, however, not realistic because of the fabrication constraints. Therefore, an optimized design with the turn width of 350 μm and gap of 150 μm was selected and implemented in this paper. It should be noted that the fabricated coils were 88 μm thick, causing the quality factor

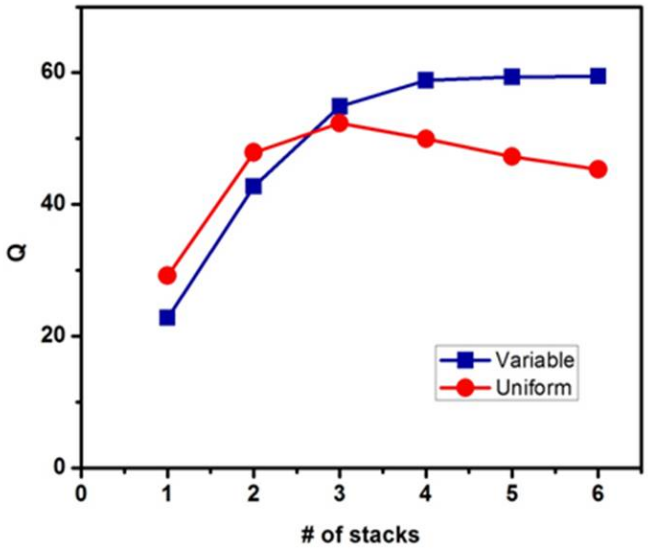


Figure 103: Simulated quality factor vs. number of parallel-connected stacked layers for uniform and variable width design at 300 kHz.

to be smaller than the simulated values presented in Table 7.

To study the effectiveness of multilayer lamination in improving quality factor, simulations for parallel-connected inductors with various numbers of lamination layers were also performed. The results are given in Figure 103. The Q-factor of the inductor increased from approximately 20 for a single-layer inductor with varying width design to more than 55 with the added second and third laminations, showing almost 200% improvement. However, a saturating trend was observed after stacking more than 4 layers, and the improvement in quality factor upon increasing layers becomes negligible. This is largely due to the increased ac resistance of the inductor, which likely results from the increased proximity effects of the added layers, despite the fact that the DC resistance continues to decrease with additional laminations.

6.2.2.2 Planar Inductor Fabrication and Characterization

To fabricate the inductor design consisting of laminated coil layers, a low-cost fabrication process based on a flexible PCB technique was proposed, as shown in Figure 104. A commercially available flexible Kapton film with copper layer on top was first

coated with a photo-definable resist and patterned using a standard photolithography process in step (a). Wet etching was then performed in step (b) to etch away the copper exposed from the photoresist pattern and define the coil windings. Due to the isotropic characteristics of the wet etching process, the cross-section of the generated coils was more of a trapezoidal shape with curved sidewalls rather than a rectangular shape. After removal of the photoresist, electroplating was conducted in step (c) to further increase the copper thickness of the windings. Since electroplating is also an isotropic process, copper grew on top of the windings as well as on the sidewall and compensated for the possible size loss coming from previous wet etching process. After multiple single-layer coils had been fabricated, a vertically laminated inductor was completed by alignment and stacking, followed by definition of electrical interconnects between layers. Pictures of the fabricated single and multi-layer inductors are shown in Figure 105. The use of flexible PCB substrates enables not only a fast and easy process with low cost, but also an inductor with flexible and low profile, which favors space-efficient incorporation of the coils into complex systems.

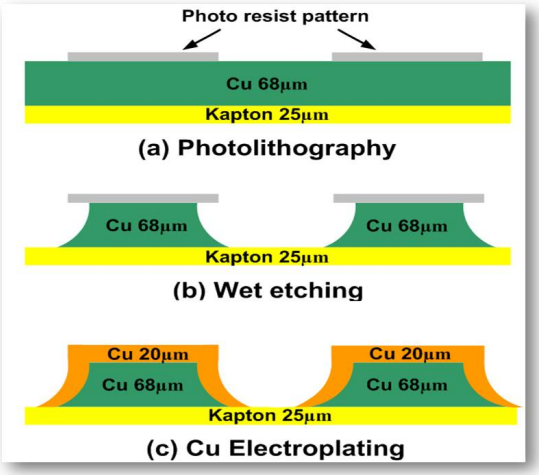
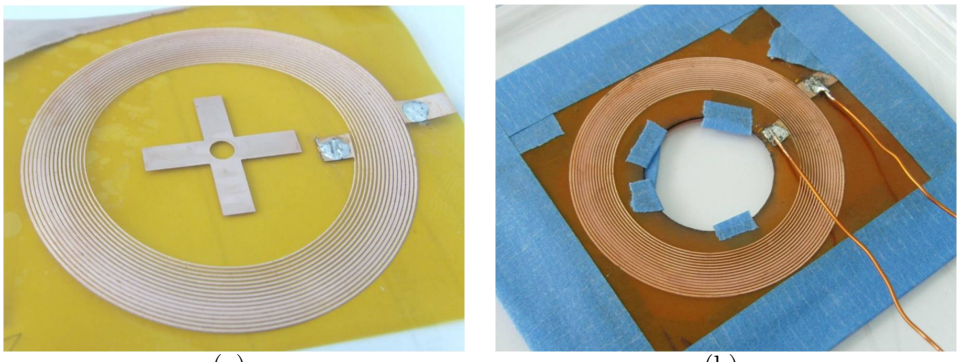


Figure 104: Fabrication process of the planar inductors using flexible PCB technique.

An impedance analyzer (HP4194) was used to characterize the resistance, inductance, and Q-factor for both single and multi-layer inductors. Results for single-layer inductors are given in Figure 106, where Coil1 to Coil4 represent four different inductors that will be laminated together. The resistance, as plotted in dashed lines, increases with frequency due to the increased eddy current loss and proximity effect at high frequencies. The measured inductance values of different coils are reasonably close and remain stable at approximately 17 μH for frequencies up to 1 MHz. The small discrepancies in values resulted from imperfectly patterned windings due to the fabrication tolerances. The Q factors reach 20 at 300 kHz and increase linearly with frequency. Characterization results for the four-layer inductor assembled using the four single-layer inductors are shown in Figure 107, where the resistance is reduced to 0.6 Ω at 300 kHz while the inductance value only experiences a small decrease from 17 μH to 16.3 μH. As a result, the Q factor reaches 50.1 at 300 kHz, which is more than two times that of the original single-layer inductors. To validate the relationship between the lamination approach and the inductor performance, the Q-factors for inductors with various laminated layers were also measured and compared with the simulation results given before, as shown in Figure 108. The three plots in the



(a) (b)

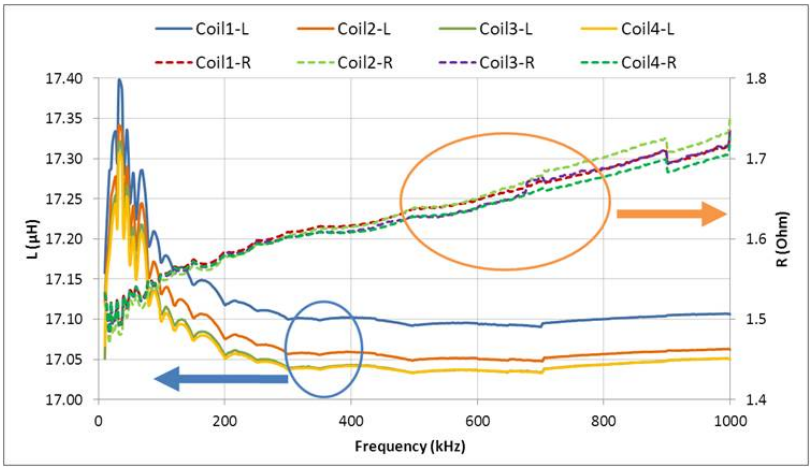
Figure 105: Fabricated spiral inductors with (a) single layer and (b) four stacked layer.

figure represent the Q-factors obtained from experimental results, previous simulation results using an ideal sidewall geometry model, and new simulation results using a trapezoidal sidewall model. As stated in the fabrication section, the cross-section of the coil winding is closer to a trapezoid rather than an ideal rectangular shape. Trapezoidal-shaped sidewalls match the experimental trend with an overall error of less than 10%. The discrepancy error mainly comes from the imperfectly fabricated devices, such as variation in winding width and gap definition, misalignment of vertical laminations, etc.

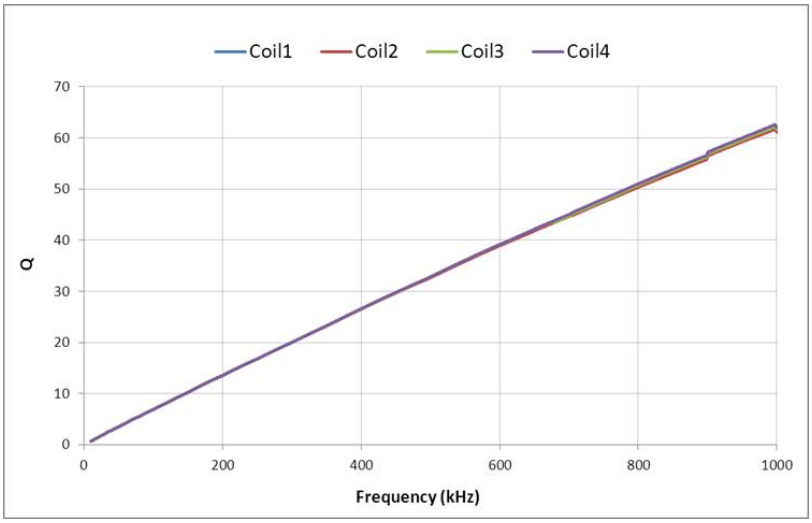
6.2.2.3 Wireless Power Transfer Testing Results

With the high Q-factor design for the receiver coil completed, the key factors remaining for enabling efficient wireless power transfer are the Q-factor of the transmitter coil and the coupling coefficient between the transmitter and receiver coil. Since the size of the transmitter coil is not as critical as the receiver coil in our application, a relatively large transmitter coil with a high Q-factor can be used. The experimental setup for resonant wireless power transfer is shown in Figure 109, which is conducted by our collaborators in National Semiconductor. On the transmitter side, an AC-DC converter is connected through an H-bridge to supply the desired ac signal from the grid, and a frequency-tuning component with control circuits is used to tune the resonant frequency of the transmitter coil. The transmitter coil is a Litz-wire coil with an outer diameter of 20 cm, an inductance value of 45.4 μH, and a high Q-factor of 847 at 300 kHz. It was automatically tuned to operate at the resonant frequency of 300 kHz with a peak voltage limit of 500 V. The multi-layer spiral inductor acts as the receiver coil with frequency tuning circuits, and voltage regulator as well as rectifier is used to deliver the power to the ultimate load. The receiver coil was manually tuned to approach the transmitter resonant frequency to maximize the power transfer efficiency.

A simplified schematic model for the system is shown in Figure 110, where V_s represents the input power source, R_s represents the resistance of the power source, C_{s1}, C_{s2}, C_{p1}, and C_{p2} are the tuning capacitances added in series or in parallel with the inductors for achieving resonance, $C_s = \frac{1}{L_s \cdot \omega_0^2}$ and $C_p = \frac{1}{L_p \cdot \omega_0^2}$, R_{Cs1}, R_{Cs2}, R_{Cp1}, and R_{Cp2} are the resistances of the corresponding capacitors, L_{s1} and L_{s2} are the leakage inductances of a transformer model representing the transmitter and receiver coil, L_p is the mutual inductance, R_1, R_2 are the resistances of the coils, and R_L is

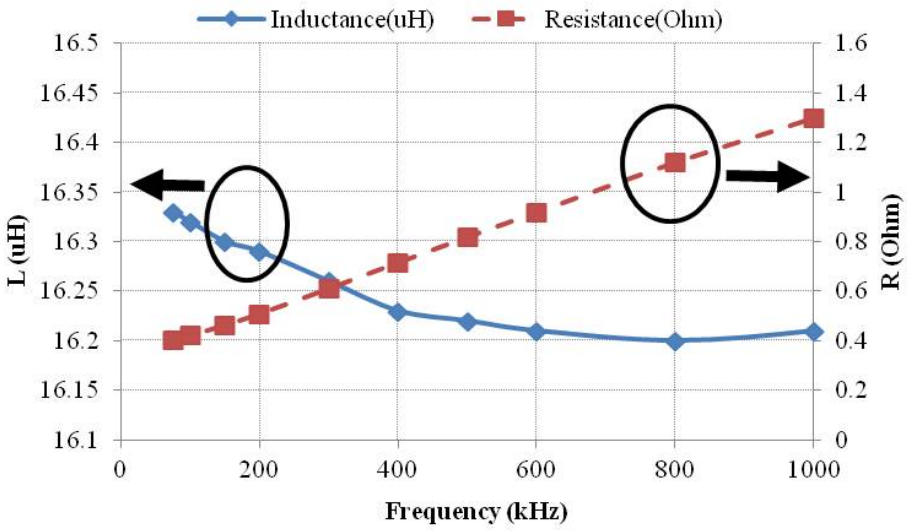


(a)

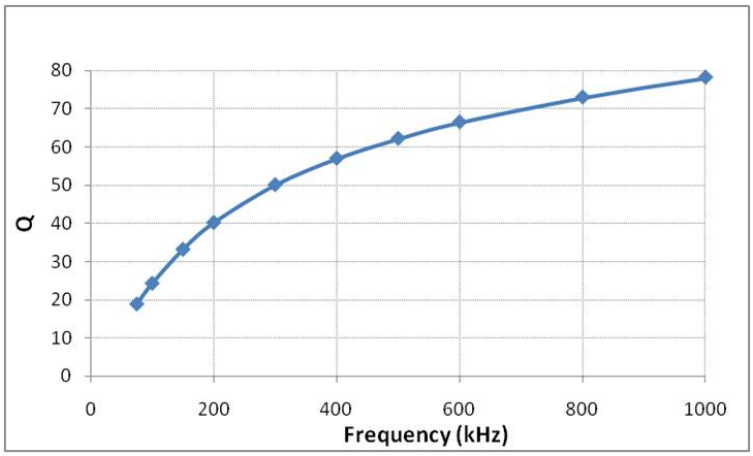


(b)

Figure 106: Characterization results for single-layer inductors, (a) inductance and resistance, (b) quality factor.



(a)



(b)

Figure 107: Characterization results for the four-layer inductor, (a) inductance and resistance, (b) quality factor.

the load resistance.

The power transfer efficiency, η_t, which describes the direct energy transfer between the transmitter and receiver coils, as discussed in equation (10), is measured as the ratio of the power received in the receiver coil to the power sent out from the transmitter coil:

$$\eta_t = \frac{V_{out} I_{out}}{V_{in} I_{in}}, \tag{24}$$

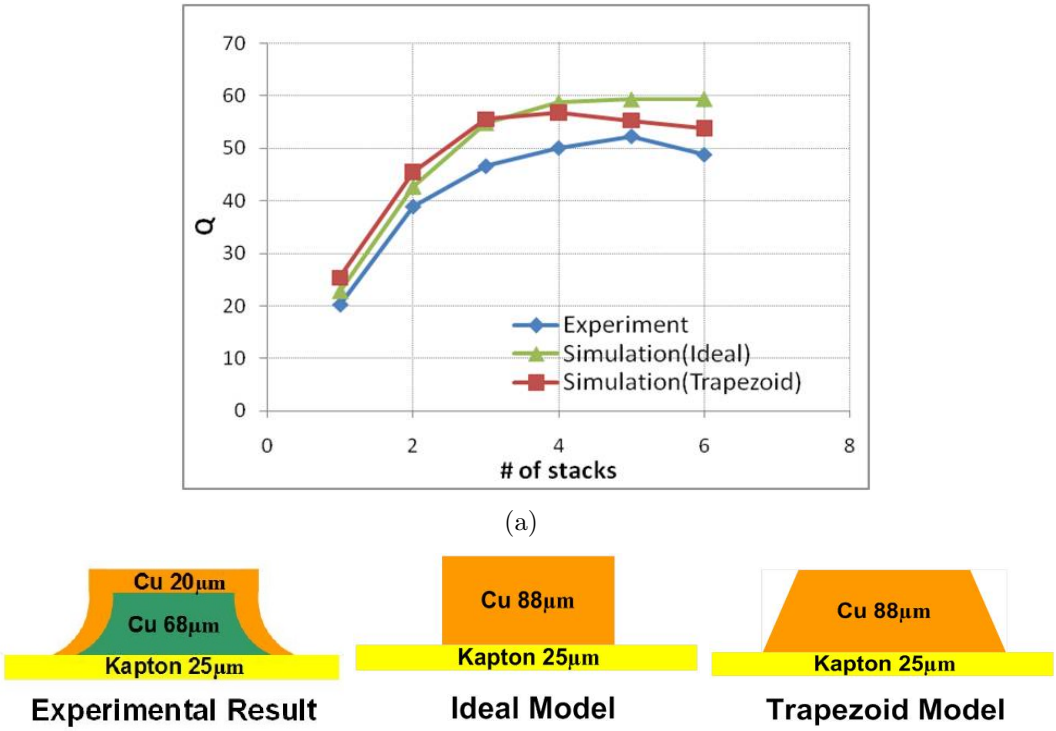


Figure 108: Measured Q-factor for various laminated layers in (a) with the simulation models shown in (b).

where V_{in} and V_{out} are the voltage labeled in Figure 110, and I_{in} and I_{out} are the current flowing in the segment corresponding to V_{in} and V_{out}.

When considering the entire system, an overall efficiency can be obtained, which describes the percentage of the power received on the load compared to the total input power from the power source.

The separation between the coils was adjustable along their axis, thus measurements were performed across an adjustable load for several different distances, with the results plotted in Figure 111. The transfer efficiency, as well as the overall efficiency, is shown as solid line with the reference axis on the left, and the actual power received on the load is shown as the dashed line with the reference axis on the right. Over a one-coil-diameter distance of 5 cm, a load power of 7 Watts is transferred at an overall efficiency of 46%, and at a two-coil-diameter distance of 10 cm, a load power

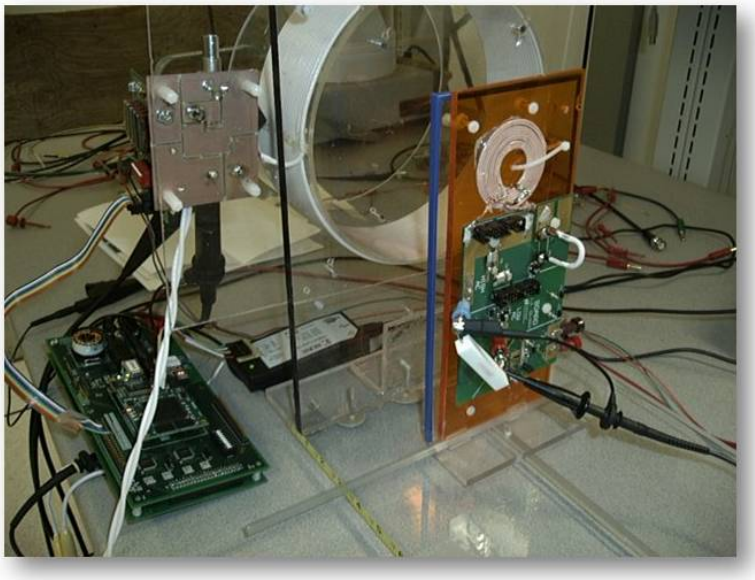


Figure 109: Experimental setup for resonant power transfer.

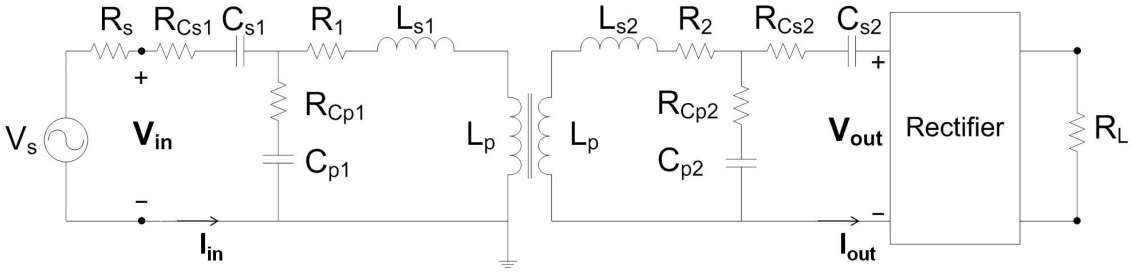


Figure 110: Schematic diagram of the test circuits for wireless power transfer.

of more than 5 Watts is successfully transferred, with an overall efficiency of 23% and a transfer efficiency of 33%. As the distance increases, the efficiency reduces, and at the distance larger than 20 cm, the efficiency drops to less than 5%. In comparison, a Litz-wire receiver coil with the same characteristics was also tested under similar conditions, and the results are shown in Figure 112, where an overall efficiency of 58% and 39% are demonstrated at one and two-diameter distances respectively.

The coupling efficient between the transmitter and multi-layer receiver coil was

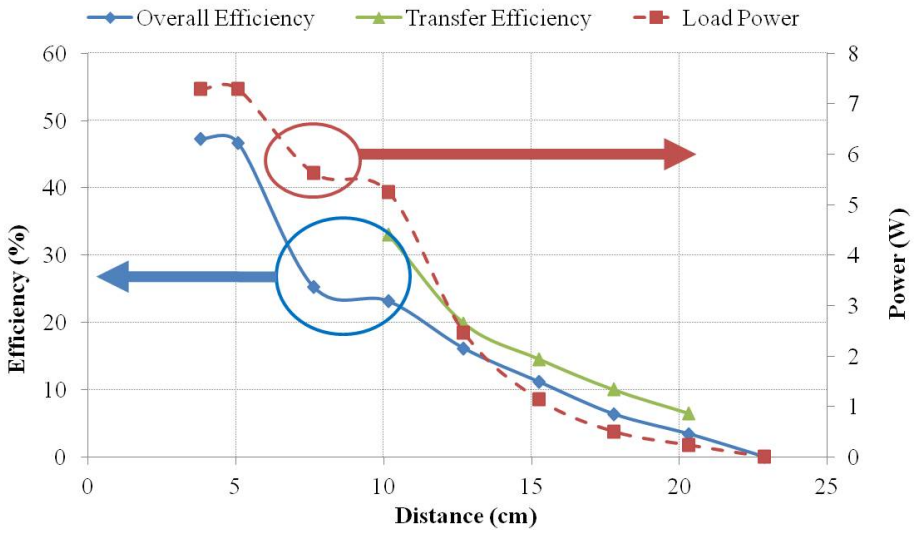


Figure 111: Measured load power, overall efficiency, and transfer efficiency for the multi-layer receiver coil.

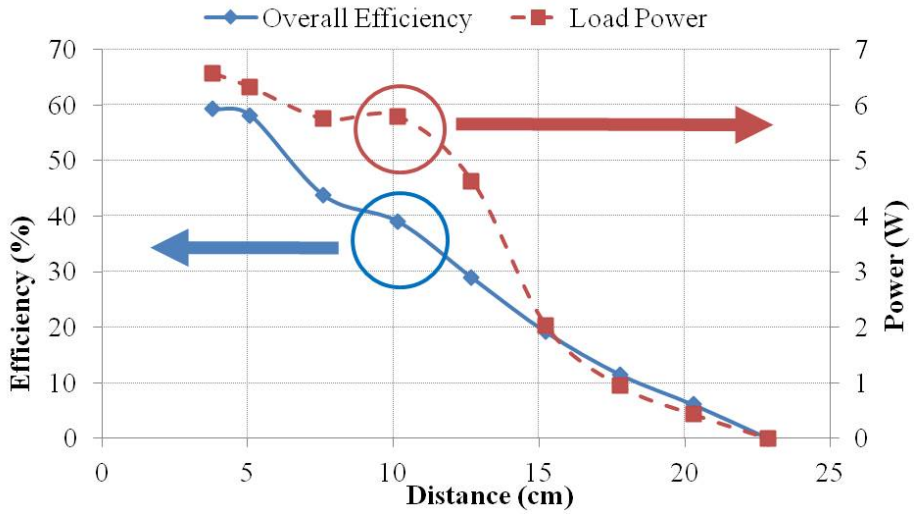


Figure 112: Measured load power and overall efficiency for the Litz-wire receiver coil.

also calculated from the measurement data using:

$$k = \frac{M}{\sqrt{L_1 L_2}} = \frac{V_{2,pk}}{\omega_0 I_{1,pk} \sqrt{L_1 L_2}}, \tag{25}$$

where ω_0 is the resonant frequency, M is the mutual inductance, $V_{2,pk}$ is the peak voltage measured in the receiver coil, and $I_{1,pk}$ is the peak current measured in the

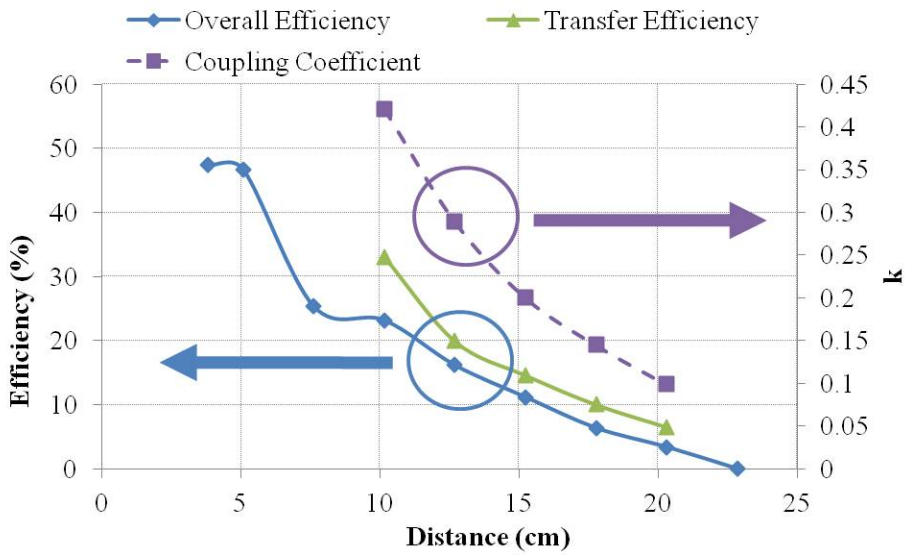


Figure 113: Measured overall efficiency, transfer efficiency and the coupling coefficient for the multi-layer receiver coil.

transmitter coil. A coupling coefficient of 0.42 was obtained at the distance of 10 cm, and 0.2 at the distance of 15 cm, as shown in Figure 113.

6.2.3 Solenoid Receiver Coil

Upon demonstrating the wireless power transfer with a Kapton-based planar coil that has a relatively large size, shrinking of the size of the receiver coil is explored. The problem with size reduction of the receiver coil is that, it is usually accompanied by a reduction in the coil inductance, quality factor and coupling coefficient, which will lead to a degradation in the power transfer efficiency as a result. The theoretical analysis behind it for a simplified case of having two coupled coils is summarized in [94] and could provide some general insights into the problem.

In the case of two circular inductors aligned and coupled as shown in Figure 114, the mutual inductance between them can be determined using the following equation [95]:

$$M = \frac{\mu\pi N_1 N_2 r_1^2 r_2^2}{2\sqrt{(r_1^2 + x^2)^3}}, \tag{26}$$

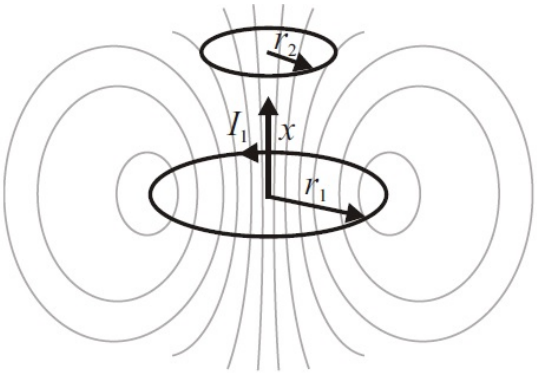


Figure 114: Representation of two coupled circular inductors.

where N_1 is the turn number in coil 1 and N_2 is the turn number in coil 2, r_1 is the radius of coil 1 and r_2 is the radius of coil 2, and x is the distance between the coupled coils.

An approximation of the inductance of the coil can be found in [96] when the multiple turns of the coil are located in close proximity to each other:

$$L = N^2 L_0 = N^2 \cdot 1.257 \cdot r[2.303 \cdot log_{10}(\frac{16r}{d} - 2)] \cdot 10^{-6}. \tag{27}$$

Substituting equation (26) and (27) into equation (25), the coupling coefficient between the two coils becomes:

$$k = \frac{\mu\pi N_1 r_1^2}{\sqrt{L_1} \cdot 2\sqrt{(r_1^2 + x^2)^3}} \cdot \frac{N_2 r_2^2}{\sqrt{L_2}}, \tag{28}$$

$$L_2 = a \cdot r_2 \cdot log_{10}(\frac{16r_2}{d} - 2), \tag{29}$$

$$a = 1.257 \cdot 2.303 \cdot 10^{-6}. \tag{30}$$

Apparently from equation (28), for a given transmitter coil and a fixed distance between the transmitter coil and the receiver coil, reducing the size of the receiver coil (r_2) would reduce the coupling coefficient between the two coils and the inductance as well according to equation (29), consequently its quality factor. Based on equation (14) for calculating the power transfer efficiency, a decrease in the transferring efficiency is therefore expected.

To maintain a high quality factor and a good coupling with the transmitter coil despite the size shrinking of the receiver coil, magnetic materials with high permeability can be used in the receiver coil to compensate for the effect of the size reduction. To also improve the flux linkage between the transmitter and receiver coil, a solenoid type receiver coil and transmitter coil is employed. Solenoid coils are better at picking up the magnetic flux in a specific direction compared to planar coils although it is not as quite good in other directions. However, special designs comprising multiple solenoid coils can be utilized if the flux collection in more directions are desirable.

In this section, we designed a low-profile solenoid inductor with a laminated CoNiFe core as the receiver coil, as shown in Figure 115. Magnet wires (red, AWG 32) are wound tightly onto a CoNiFe core that is housed by a laser-cut bobbin structure (blue) to form the windings of a solenoid inductor. The cross-sectional area of the solenoid windings is approximately 300 μm by 2 mm. The laminated CoNiFe core (green) is developed by our group and details about the material and its fabrication

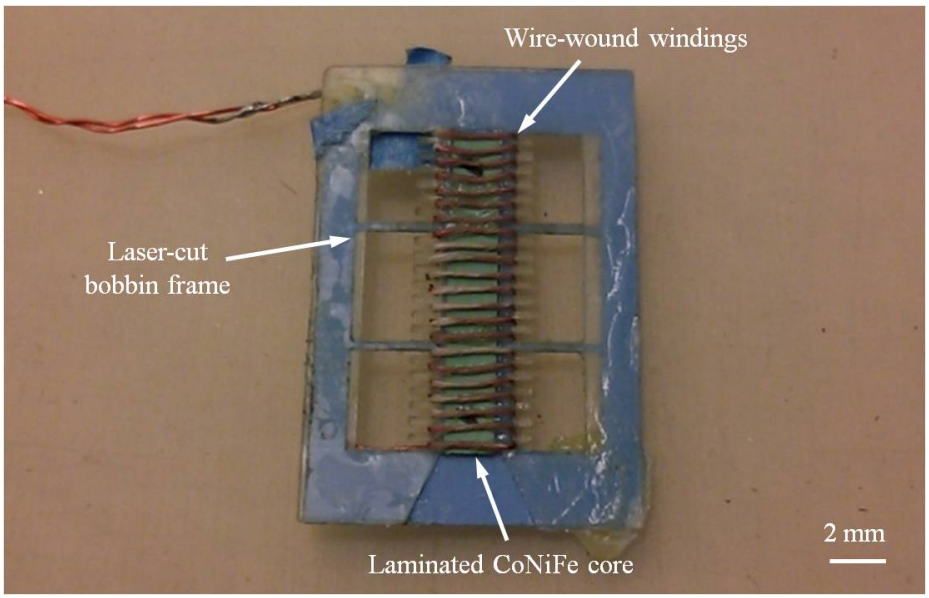


Figure 115: Photograph of the designed solenoid receiver coil with laminated CoNiFe core.

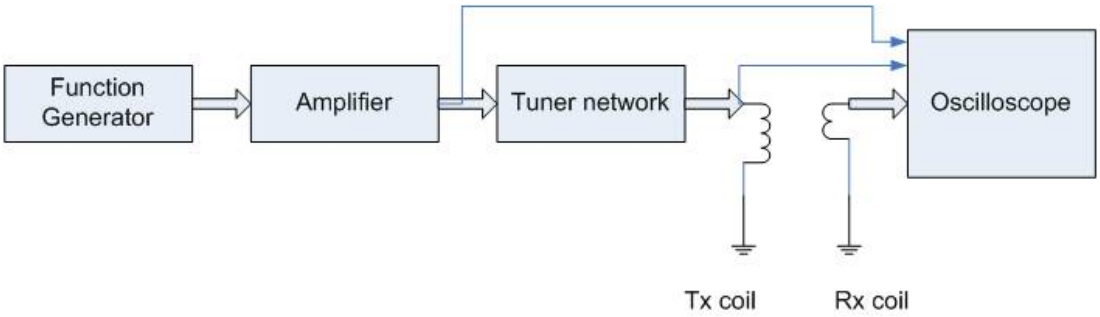


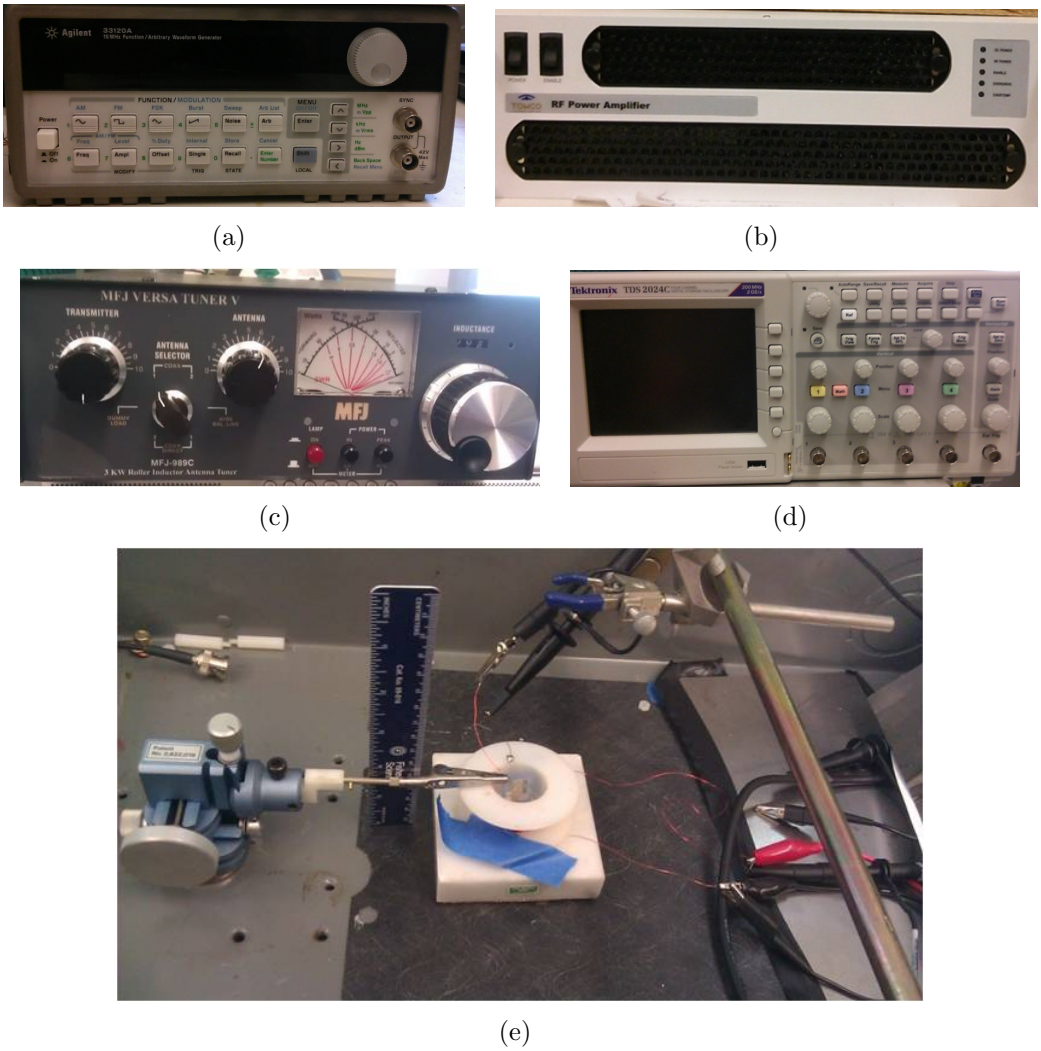
Figure 116: Schematic of the experimental setup for testing wireless power transfer with low-profile solenoid receiver coils.

process can be found in [97]. It has a permeability of approximately 200 and is composed of 70 insulated layers of 500-nm-thick CoNiFe. The total effective thickness of the magnetic material, therefore, is approximately 35 μm. The lateral dimension of the core is approximately 2 mm by 15 mm. For comparison, a solenoid air-core coil is also wound using magnet wires with the same geometry.

The experimental setup for testing the wireless power transfer using the presented solenoid receiver coil comprises a signal generator, a RF power amplifier, a tuner network, and an oscilloscope in addition to the transmitter coil and receiver coils, as shown in Figure 116. The signal generator drives a sinusoidal voltage into the power amplifier at a desired frequency and amplitude. The output of the amplifier is connected to the transmitter coil through a tuner network, which provides impedance matching between the two and maximize the power delivery to the transmitter coil from the amplifier. The current of the transmitter coil is picked up by a current probe (Tecktronix) and is sent to the oscilloscope, together with the voltage of the transmitter coil and the receiver coil. Current monitoring ensures a consistent magnetic field to be provided by the transmitter coil and the voltage generated on the receiver coil can be read directly from the oscilloscope. Details of the equipment used in the experimental setup is shown in Figure 117. The coupled transmitter and receiver coil is placed in a metal box which works as a shield during wireless power transfer

for safety purposes. The receiver coil is held by a clamp on top of the receiver coil, the position of which is controlled by a motor. The metal clip shown in the picture is switched to plastic ones during the actual measurements in order to avoid any interference on the testing results.

The transmitter coil is a solenoid inductor wound with magnet wires (AWG 32) that has a coil radius of approximately 2.6 mm and a height of 3 mm. It exhibits an



(a) (b) (c) (d) (e)

Figure 117: Photograph of the equipments and coils in the experimental setup: (a) functional generator, (b) high-power amplifier, (c) tuner network for impedance matching, (d) oscilloscope, and (e) the coupled transmitter and receiver coils, which is held by a clip.

inductance of 8 μH, a DC resistance of approximately 0.662 Ω and a quality factor of 140 at 9 MHz, as can be seen from the characterization results shown in Figure 118. Besides, the transmitter coil resonates at approximately 30 MHz.

Characterization results of the solenoid receiver coil with the laminated core is shown in Figure 119, demonstrating an inductance of 368 nH and a quality factor of 18 at approximately 7 MHz. In comparison, an inductance of 84 nH is measured for the air-core solenoid with a quality factor of 14 at 7 MHz. Obviously the inductance

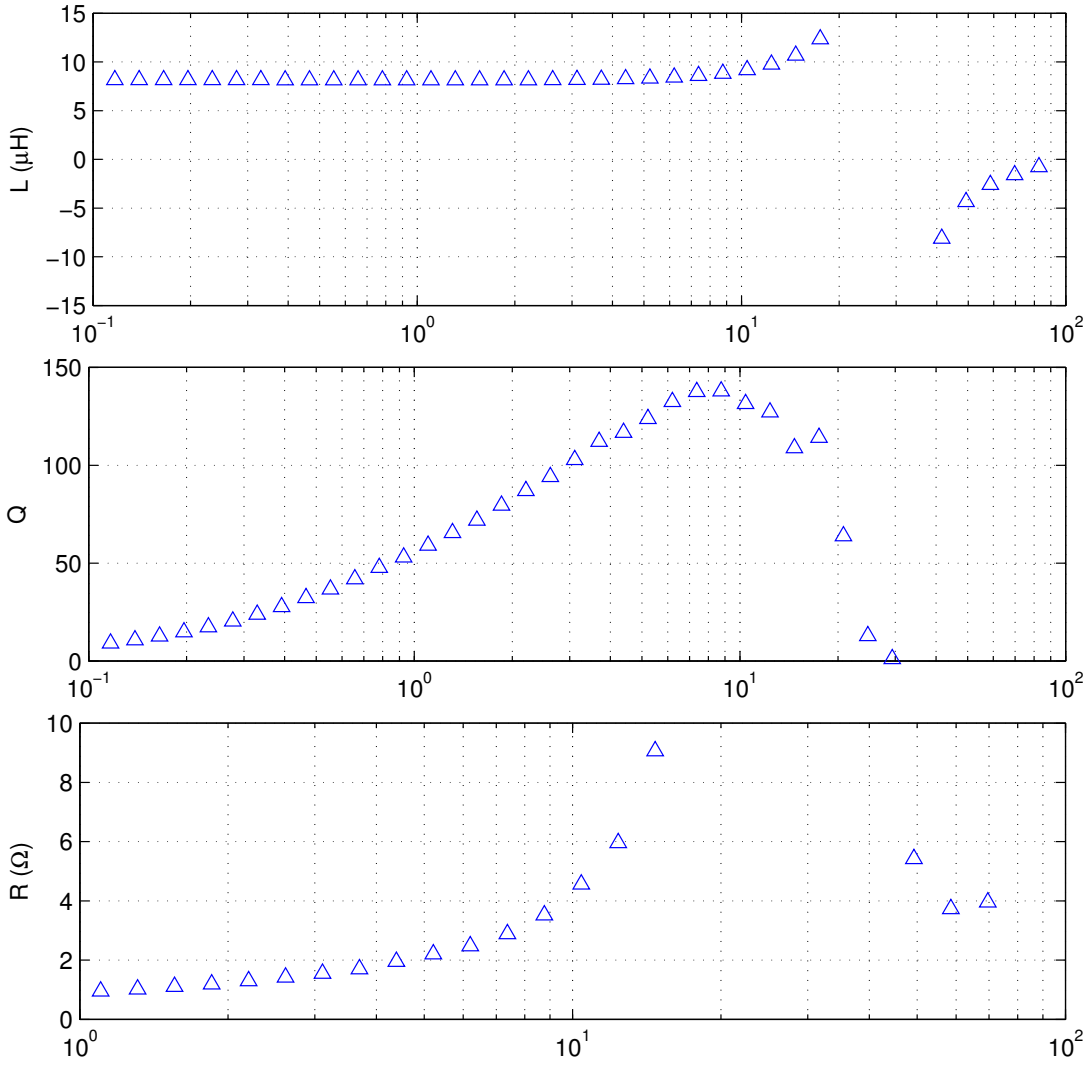


Figure 118: Measured inductance (L), quality factor (Q), and resistance (R) of the solenoid transmitter coil.

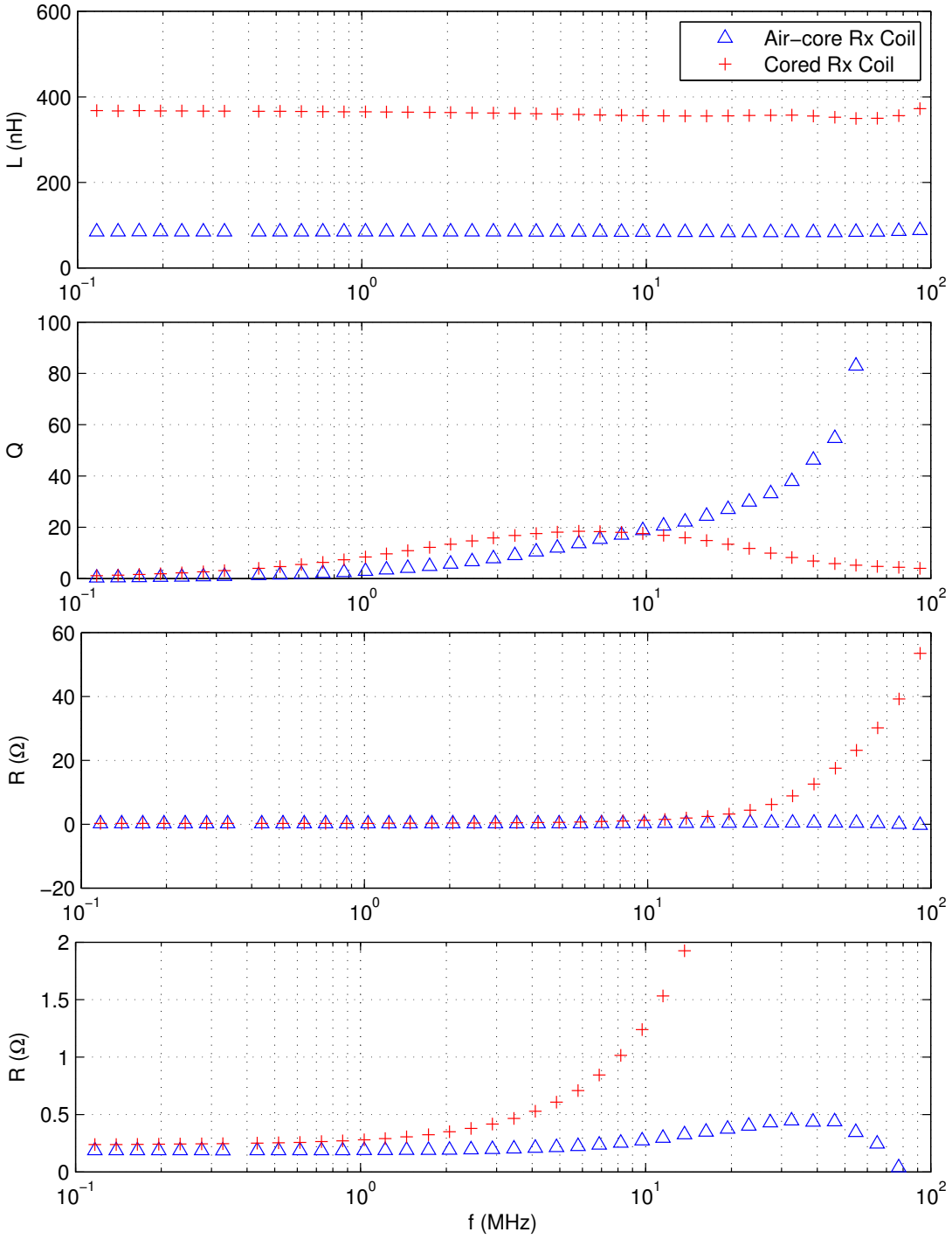


Figure 119: Measured inductance (L), quality factor (Q), and resistance (R) of the solenoid receiver coils.

of the receiver coil is boosted by a factor of 4 by employing the thin magnetic core and its qualify factor also sees an increase. Experiments are then conducted to explore the

effect of having high-permeability materials in improving the power transfer efficiency.

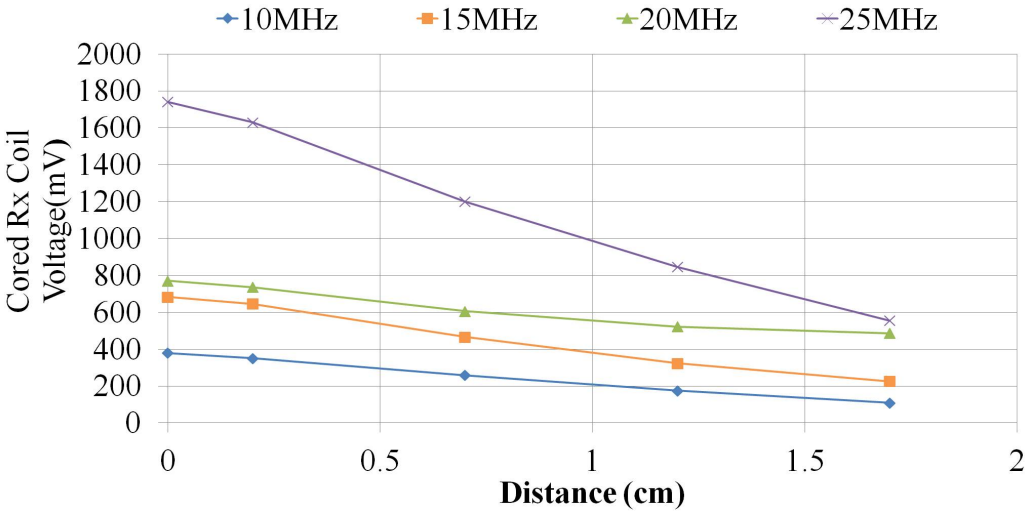
Results of transferring power between the proposed transmitter coil and receiver coils are shown in Figure 120. The current in the transmitter coil is set to be 600 mA (RMS value) and the power transfer at various frequencies from 10 MHz - 30 MHz is tested. The definition of the origin of the distance between the transmitter coil and the receiver coil, as shown in the x axis of the testing results, is illustrated in Figure 122. Photograph of the typical signal waveforms captured by the oscilloscope during wireless power transfer is shown in Figure 123, including the transmitter voltage, current and the generated receiver voltage.

As can be seen from Figure 120, first, the voltage induced in the receiver coil is the largest at the closest distance, and it drops monolithically with increasing separation between the coupled coils. Second, the induced voltage also increases with increasing frequency and is boosted at 30 MHz when resonance of the transmitter coil happens, which can be seen from the testing results of the air-core solenoid. The power transfer at 30 MHz using the magnetic-core solenoid could not be completed due to the signals overloading the amplifier. Third, the induced voltage on the solenoid receiver coil with magnetic core is approximately 4 times the voltage on the air-core receiver coil, which justifies the benefit of having a magnetic core to boost the inductance and coupling of the receiver coil for a better power transfer efficiency.

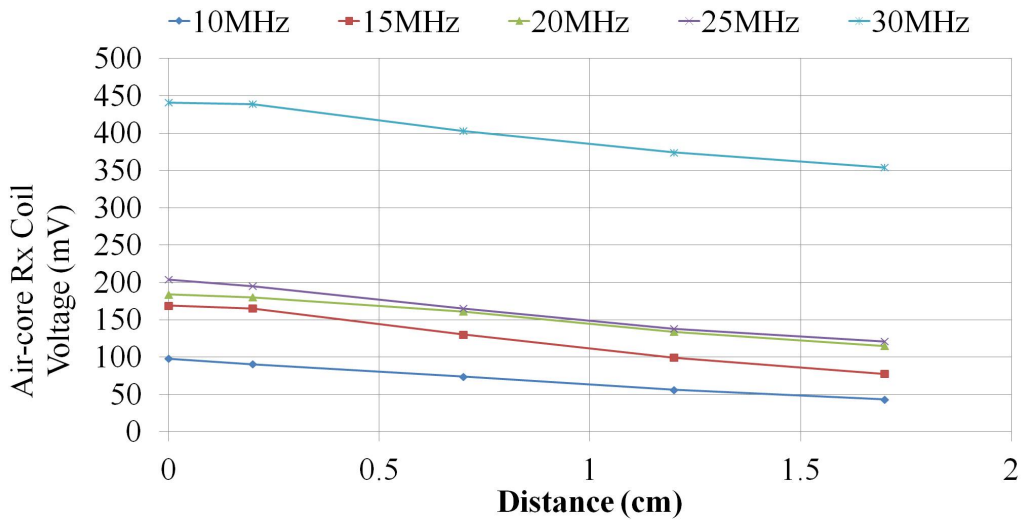
Results of transferring power at lower frequencies from 5 MHz to 10 MHz with a transmitter current of 900 mA is also shown in Figure 124. Since the solenoid magnetic-core receiver coil has a higher quality factor than the air-core receiver coil in this range, the generated voltage with magnetic core is more than 6 times that of the air-core receiver coil.

6.2.4 Summary

In this section pertaining to wireless power transfer, a macro-sized planar receiver coil is first developed to demonstrate the resonant power transfer. Then as an effort towards realizing micro-sized receiver coil, a low-profile solenoid receiver coil is developed. To compensate for the performance degradation that intrinsically accompanies



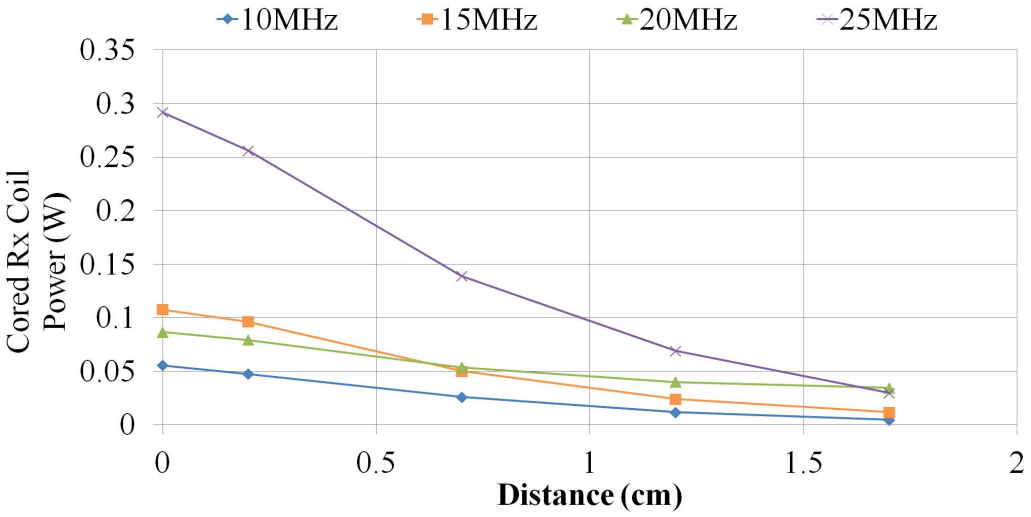
(a)



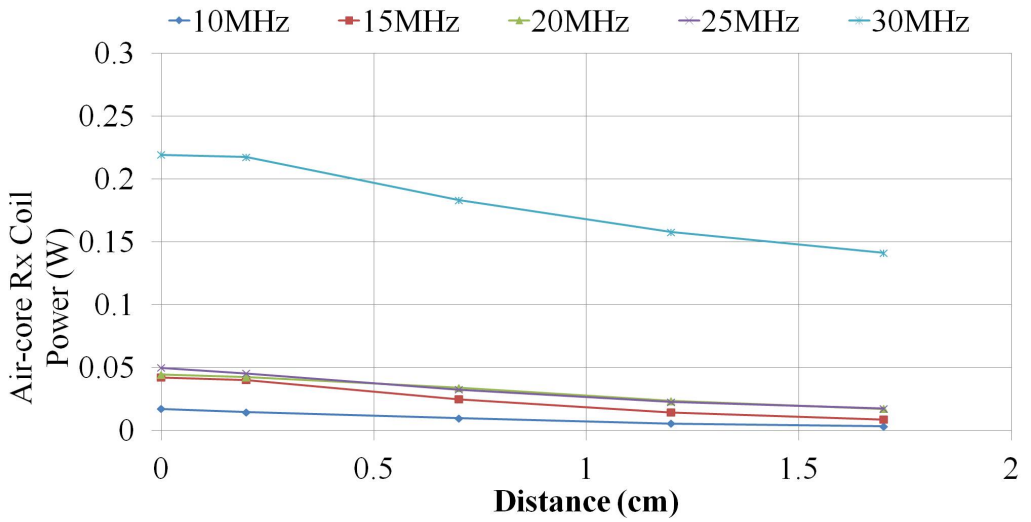
(b)

Figure 120: Measured voltage on the receiver coil when $I_{tx\_coil} = 600mA$: (a) solenoid with laminated CoNiFe core, and (b) air-core solenoid.

with size reduction of the receiver coil, high-permeability magnetic material is employed in the solenoid receiver coil and demonstrated to be capable of improving the coupling and inductance of the receiver coil and consequently the power transfer efficiency. These preliminary efforts makes promising the future of using integrated and miniaturized silicon-embedded components in wireless power transfer while achieving



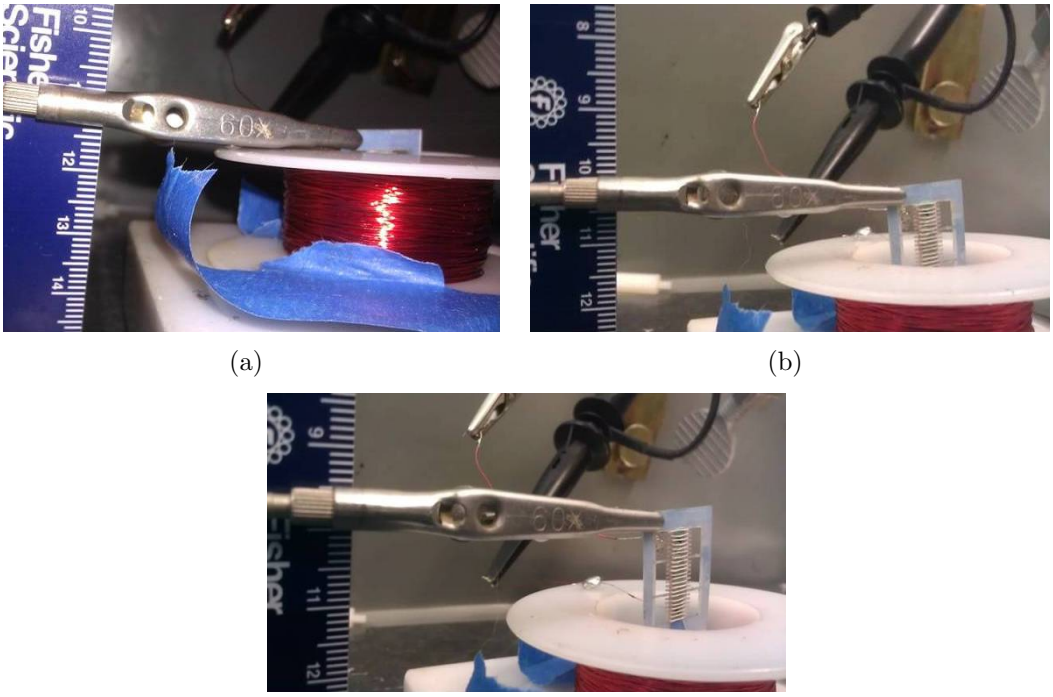
(a)



(b)

Figure 121: The maximum power deliverable to the receiver coil when $I_{tx\_coil} = 600mA$: (a) solenoid with laminated CoNiFe core, and (b) air-core solenoid.

a satisfactory performance.



(a) (b)

(c)

Figure 122: The defined position of the receiver coil relative to the transmitter coil, (a) distance 0, (b) distance at the mid point, and (c) furthest distance.

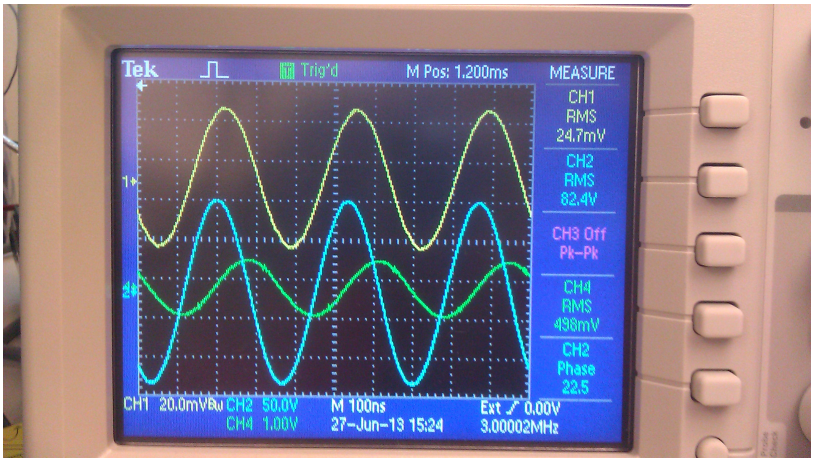
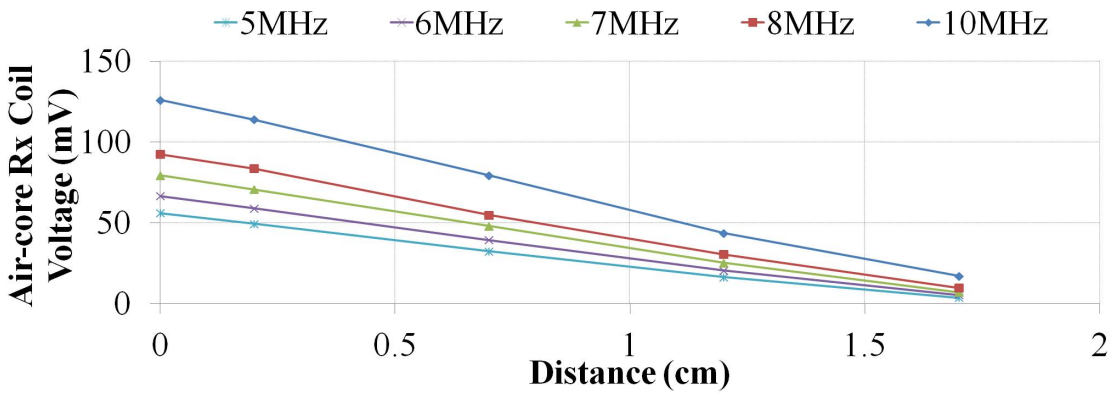
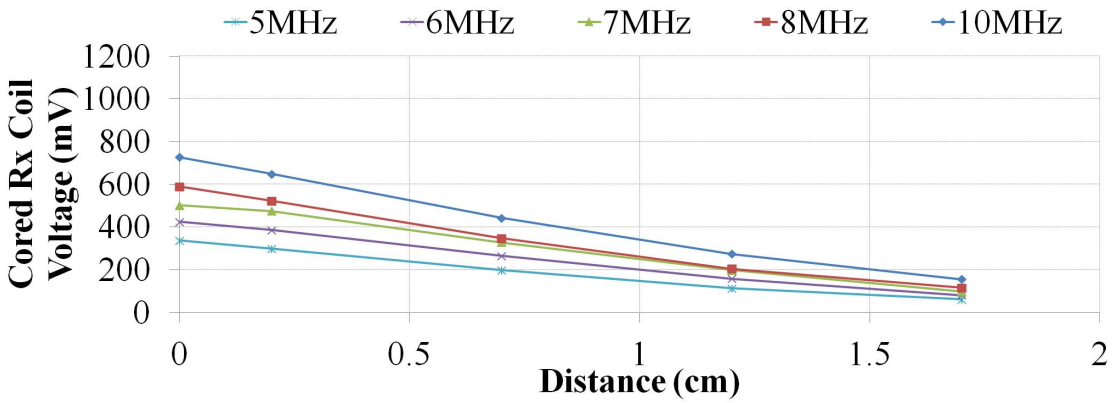


Figure 123: Measured waveform of the output signals on the oscilloscope including transmitter voltage, current and receiver voltage.



(a)



(b)

Figure 124: Measured voltage on the receiver coils when $I_{tx\_coil} = 900mA$: (a) air-core solenoid and (b) solenoid with laminated CoNiFe core.

CHAPTER VII

CONCLUSION

7.1 Summary of Conducted Research

In accordance with the objective of our proposed research, we have demonstrated the advanced fabrication technologies for silicon embedding and as an example that could benefit from using embedded structures, how to design, fabricate, characterize, and test silicon-embedded magnetic components for on-chip integrated power applications.

In chapter 3, two fabrication technologies for realizing silicon embedding of 3-D toroidal inductors are presented, including the lithography-based approach and the 3-D shadow mask-based approach. The lithography-based approach employs conventional well-developed technologies such as spray coating of photoresist, proximity lithography, thick epoxy patterning and dry-film lithography to create the 3-D toroidal inductors in deep silicon trenches in a sequentially layer-by-layer approach. Patterning on the sidewall of the trenches is avoided since conducting lithography on vertical sidewalls is extremely challenging. The 3-D shadow-mask approach, however, enables direct sidewall patterning by combining the use of a 3-D silicon shadow mask with DRIE technology that forms recessed patterns on the trench sidewall. It reduces processing complexity and saves processing time due to the elimination of multiple lithography steps, thick epoxy patterning steps and lengthy electroplating steps as in lithography-based approach. Through-wafer interconnects are demonstrated with an integration process that is compatible with both embedding approaches. Incorporating magnetic cores to enhance the performance of the toroidal inductors is also demonstrated by employing a drop-in approach. To further improve the inductance density within the limited footprint, a double-layer winding technology that is

developed based on the 3-D shadow-mask approach is also presented.

In chapter 4, since the required inductor characteristics depend strongly on the circuit topology and performance requirements, our target power converter circuit for driving LED lights are first introduced. To design inductors with desired performance as determined by the circuit, the complicated loss mechanisms in the embedded inductors across a wide frequency range are explored through a distributed equivalent circuit model upon understanding the microfabrication constraints that are imposed on the embedded toroidal inductors based on the fabrication technologies that we developed. Design and optimization strategy for the silicon-embedded toroidal inductors are then developed to deal with the trade-offs between design parameters and help guide the exploration in the design space for optimized performance based on the relative significance between various loss mechanisms in the inductor. Examples of using the inductor design and optimization strategy are also presented.

In chapter 5, both air-core and magnetic-core silicon-embedded toroidal inductors are fabricated following the proposed embedding technologies and characterized using an impedance analyzer, demonstrating inductances from 45 nH to over 1 μH and quality factors of as high as 37 at 10 MHz within limited footprints. These inductors are then tested in our targeted DC-DC power converter circuit that works with a wide range of high input voltages (25-200 V) and delivers a medium-level power (tens of watts) to drive LED lights at an output voltage of 35 V. The fabricated inductors with iron powder cores are verified to provide sufficient inductances and quality factors to enable the converter circuit to operate at an efficiency above 91% at a maximum input voltage of 100 V with a switching frequency of approximately 8 MHz.

In chapter 6, preliminary efforts in exploring silicon-embedded components for other integrated power applications are also presented. Silicon-embedded transformers are fabricated based on the processing technology developed for realizing double-layer

winding inductors. Although fully-functional embedded transformers are not demonstrated due to the non-desired shorts between windings and our limited fabrication time, characterized performances of the fabricated transformers are still promising and the fabrication process can be optimized to eliminate the patterning imperfections (just like in the fabrication of double-layer winding inductors), which will enable a functional transformer to be achieved. Embedded solenoid inductors with high-permeability magnetic materials is deemed to be a promising solution in enabling miniaturization of the receiver coils for wireless power transfer applications. A micro-sized planar receiver coil is first developed to demonstrate the resonant wireless power transfer and then a low-profile solenoid receiver coil is developed to validate the use of high-permeability magnetic materials in improving the power transfer performance.

7.2 Contributions of This Dissertation

This dissertation presented the concept of embedding 3-D functional structures into the volume of the silicon substrates using MEMS technology, which enables a greater level of miniaturization and integration for space-constrained systems, and illustrated it with a specific example of employing silicon-embedded toroidal inductors for integrated DC-DC power converters. Four substantial contributions as a result of this research are summarized as follows:

1. Advances in fabrication technologies to realize silicon embedding of 3-D functional structures for miniaturization and integration purposes: The difficulty of patterning on deep 3-D recessed surfaces is overcome by using both a conventional lithography-based approach and a non-conventional 3-D shadow mask approach, with each possessing its own advantages and limitations. Direct patterning on vertical sidewalls, in particular, is enabled by the employment of a 3-D silicon shadow mask in combination with the DRIE technology, which allows for conformal metal deposition method that enables structures to be

obtained on 3-D recessed surfaces simultaneously. As a result, 3-D functional structures with tall profile and complex geometries are able to be embedded into the 'dead volume' of the silicon substrate without consuming valuable die area on the wafer front.

2. Advances in inductor fabrication technologies that enables double-layer windings to be manufactured in solenoid/toroidal inductors with significantly reduced steps. The simultaneous formation of conductors on 3-D recessed surfaces (along vertical sidewall and bottom surface of the silicon trench), as enabled by the 3-D silicon shadow-mask approach, in combination with the conformal parylene isolation layer, allows for overlapped layers of conductors to be fabricated, overcoming the problem of having limited patterning resolution and saving fabrication efforts.

3. Advances in demonstrating the concept of employing silicon-embedded magnetic components for achieving on-chip integrated high-frequency high-efficiency power converters to drive LED lights: 3-D toroidal inductors are fabricated using the developed embedding technologies. Inductor design, modeling and optimization is understood under the embedding constraints. The fabricated inductors within the limited footprint are characterized and tested to be able to provide the desired converter performance.

4. Exploration of using embedding technology as an alternative solution for enabling integration and miniaturization of other space-constrained systems: in addition to the realization of 3-D toroidal inductors that we presented, other silicon-embedded components such as transformers and solenoid inductors could also be realized for various applications such as isolated power converters and wireless power transfer. Preliminary experiments are conducted to explore the possibility of using miniaturized embedded components for these applications.

7.3 Future Work

With the double-layer winding technology proposed based on the silicon-embedding technology, the footprint of the embedded 3-D toroidal inductors can be further reduced while still providing sufficient inductances for circuit operation. The quality factors of these inductors can be further improved through process optimization such as electroplating thicker conductors and maximizing winding widths, which is not conducted in this dissertation. The profile of the integrated power converter system can therefore be potentially further reduced with the reduction in the inductor footprint.

Upon verifying the feasibility of employing silicon-embedded toroidal inductors for meeting the performance requirements of the integrated power converter application, the ultimate on-chip integration of power transistors and control circuits with embedded toroidal inductors can be explored for a complete system demonstration.

Silicon-embedded transformer device is a promising solution for enabling various integrated power applications such as isolated power converters. The fabrication process presented can be further optimized and improved to enable fully-functional embedded transformers to be fabricated. Characteristics of the embedded transformers can then be studied to understand its implication and limitation in various applications.

Wireless power transfer using silicon-embedded receiver coils is also a promising solution for realizing miniaturization of the power transfer system on the receiver side. Silicon-embedded receiver coils with high-permeability magnetic materials can be developed based on the embedding technology we demonstrated to enable efficient wireless power transfer. Miniaturized energy harvesting system can also be explored with realization of embedded energy harvesting components, which takes advantage of the unused silicon volume to enable a chip-scale integration of the energy harvesting system. Other components such as antennas can also be integrated into the substrate

and alternative substrates can also be explored based on the embedding technology we have demonstrated for the silicon substrate.

APPENDIX A

MEASUREMENT DATA

The detailed measurement data for Figure 120 is in the Table 8 and Table 9. Multiplying Channel 1 result by 10 mA/mV gives the current in the transmitter coil. Channel 2 of the oscilloscope measures the voltage on the receiver coil. Channel 3 measures the voltage on the transmitter coil. What Channel 4 measures is only a portion of the output voltage of the amplifier. All the measure data are RMS values. The detailed measurement data for Figure 124 is in the Table 10 and Table 11.

Table 8: Measurement Data for the Cored Solenoid Receiver Coil at a Transmitter Coil Current of Approximately 600 mA

Laminated 10 MHz core		Oscilloscope				
Relative Distance (cm)	FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
1.7	-31	57.7	28.9	111	109	0.0046
1.2	-31	57.3	29.4	117	175	0.0118
0.7	-31	57	29.1	113	259	0.0259
0.2	-31	56.5	29.1	112	351	0.0476
0	-31	56.8	29	116	379	0.0555

15 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx curent (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-24.5	57.9	45.5	1130	225	0.0117
-24.5	57.5	45.6	1120	323	0.0241
-24.5	57.3	45.6	1130	466	0.0501
-24.5	57.3	46.2	1130	646	0.0963
-24.5	57.3	45.7	1400	683	0.1077

20 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-18	72.5	55.8	3560	486	0.035
-18	72.1	55.6	3580	522	0.04
-18	68.7	54.3	3590	606	0.054
-18	68.2	54.9	3310	736	0.079
-18	68.4	55.4	3340	770	0.087

25 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-15	71.4	102	1890	555	0.03
-15	70.4	103	1970	846	0.07
-15	69.2	102	1990	1200	0.14
-15	69	101	1870	1630	0.26
-15	68.2	103	1980	1740	0.29

Table 9: Measurement Data for the Air-Core Solenoid Receiver Coil at a Transmitter Coil Current of Approximately 600 mA

freq (MHz)	**Air core**	10 MHz		Oscilloscope			
Distance (cm)	Distance (cm)	FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
6	1.7	-30	60.1	30.8	141	43.2	0.0034
5.5	1.2	-30	59.2	31	140	56.1	0.0057
5	0.7	-30	59.7	31.1	136	73.9	0.0099
4.5	0.2	-30	59.4	30.6	139	90.4	0.0148
4.3	0	-30	58.7	30.6	135	98	0.0174

15 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-24	58.1	45.8	1270	77.6	0.00894
-24	58	45.9	1260	99.1	0.01458
-24	57.7	46.2	1280	130	0.02508
-24	57.7	46.6	1310	165	0.04041
-24	59.2	46.1	1300	169	0.04239

20 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-23	62.9	33.5	2330	115	0.01741
-23	62.6	33	2190	134	0.02364
-23	61.7	32.7	2400	161	0.03412
-23	58.9	30.8	2180	180	0.04265
-23	57.1	30.4	2270	184	0.04457

25 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-23	60.9	34.2	2470	121	0.0176
-23	59.7	34	2530	138	0.0229
-23	60.7	33.7	2510	165	0.0327
-23	61.3	33.3	2490	195	0.0457
-23	60.7	32.3	2500	204	0.05

30 MHz		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-21	68.2	34.8	924	354	0.1414
-21	64.9	35.4	920	374	0.1578
-21	62	35.4	904	403	0.1832
-21	60.6	36	876	439	0.2174
-21	59.7	35.7	869	441	0.2194

Table 10: Measurement Data for the Cored Solenoid Receiver Coil at a Transmitter Coil Current of Approximately 900 mA

Laminated 10 core		Oscilloscope				
Distance (cm)	FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
1.7	-27	91.8	47	182	178	0.012234
1.2	-27	91.4	46.7	180	282	0.030707
0.7	-27	91.5	46.8	187	421	0.068438
0.2	-27	91	46.5	180	581	0.130342
0	-27	90.4	46.4	184	624	0.15035

15		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-20	89.4	71.6	1800	352	0.02859
-20	89.5	71.4	1750	513	0.06073
-20	89	72.1	1760	740	0.12637
-20	89.2	72.2	1760	1020	0.2401
-20	89.3	72.6	2260	1090	0.27419

20		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-15	86.7	81.1	4410	488	0.03479
-15	85.1	81.1	4320	528	0.04073
-15	92.3	80	5200	707	0.07302
-15	91.5	79.8	4830	847	0.10481
-15	91.6	79.4	4850	885	0.11442

Table 11: Measurement Data for the Air-Core Solenoid Receiver Coil at a Transmitter Coil Current of Approximately 900 mA

Air core	10		Oscilloscope			
Distance (cm)	FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
1.7	-26	94.4	49.1	222	66	0.007886
1.2	-26	94	49	218	86.8	0.013639
0.7	-26	93.6	49.2	219	116	0.024359
0.2	-26	93.4	48.9	215	144	0.037538
0	-26	93	48.2	211	154	0.042933

15		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-20	90	71.6	1910	121	0.02173
-20	90.3	71.9	1990	155	0.03566
-20	90.2	72.5	1990	202	0.06056
-20	90.8	72.7	2030	256	0.09726
-20	90.6	72.5	2040	264	0.10344

20		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-20	87.5	47.5	3310	163	0.03498
-20	88	46.8	3170	186	0.04555
-20	88.3	46.4	3300	227	0.06784
-19	97.2	48.8	3490	284	0.10618
-19	91.6	48	3600	290	0.11072

25		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-19	93.8	53.8	3850	187	0.042
-19	94.6	53.9	3960	219	0.0576
-19	95.5	53.4	3960	263	0.0831
-19	96.7	52.8	4010	307	0.1132
-19	96.3	52.8	4000	328	0.1292

30		Oscilloscope			
FunGen (dB)	Ch1 Tx current (mV)	Ch3 Tx coil (V)	Ch4 Amp output (mV)	Ch2 Rx coil (mV)	Max power (W)
-18	97.1	49.6	1270	500	0.282
-18	91.9	50.3	1250	524	0.3098
-18	88	50.4	1270	573	0.3704
-17	96.8	57.3	1430	633	0.452
-17	93.2	57.3	1350	683	0.5263

REFERENCES

[1] Texas Instruments, *Design Summary for MicroSiP^{TM}-enabled TPS8267xSiP*. www.ti.com/lit/ug/slib006/slib006.pdf, 2011.

[2] P. Hazucha, G. Schrom, J. Hahn, B. Bloechel, P. Hack, G. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 4, pp. 838–845, April 2005.

[3] W. Zhang, M. Wilkowski, J. Weld, and A. Lotfi, "A 20MHz monolithic DC-DC converter manufactured with the first commercially viable silicon magnetics technology," in *Power Electronics and Motion Control Conference (IPEMC), IEEE 7th International*, vol. 1, June 2012, pp. 705–712.

[4] K. H. Kim, J. Kim, H.-J. Kim, S. H. Han, and H. J. Kim, "A megahertz switching DC/DC converter using FeBN thin film inductor," *Magnetics, IEEE Transactions on*, vol. 38, no. 5, pp. 3162–3164, Sep 2002.

[5] M. Yamadaya, M. Owa, and H. Matsuo, "A boost type embedded inductor DC-DC converter with small-size and high efficiency," in *Power Electronics Specialists Conference (PESC2008)*, Jun 2008, pp. 1028–1032.

[6] H. Bergveld, K. Nowak, R. Karadi, S. Iochem, J. Ferreira, S. Ledain, E. Pieraerts, and M. Pommier, "A 65-nm-CMOS 100-MHz 87%-efficient DC-DC down converter based on dual-die system-in-package integration," in *Energy Conversion Congress and Exposition (ECCE)*, Sept 2009, pp. 3698–3705.

[7] M. Wang, J. Li, K. D. T. Ngo, and H. Xie, "A surface-mountable microfabricated power inductor in silicon for ultracompact power supplies," *Power Electronics, IEEE Transactions on*, vol. 26, no. 5, pp. 1310–1315, May 2011.

[8] I. Park, S. Kim, J. Koo, T. Roh, D. W. Lee, Y. Yang, and J. Kim, "A fully integrated thin-film inductor and its application to a DC-DC converter," *ETRI Journal*, vol. 25, no. 4, pp. 270–273, Aug 2003.

[9] Y. Katayama, S. Sugahara, H. Nakazawa, and M. Edo, "High-power-density MHz-switching monolithic DC-DC converter with thin-film inductor," in *Power Electronics Specialists Conference, IEEE 31st Annual*, vol. 3, Jun 2000, pp. 1485–1490.

[10] W. R. and J. Sin, "A novel silicon-embedded coreless inductor for high-frequency power management applications," *Electron Device Letters, IEEE*, vol. 32, no. 1, pp. 60–62, Jan 2011.

[11] T. Pan, A. Baldi, E. Davies-Venn, R. Drayton, and B. Ziaie, "Fabrication and modeling of silicon-embedded high Q inductors," in *Micro Electro Mechanical Systems (MEMS), 17th IEEE International Conference on*, Jan 2004, pp. 809–812.

[12] Y.-C. Liang, W. Zeng, P. H. Ong, Z. Gao, J. Cai, and N. Balasubramanian, "A concise process technology for 3-D suspended radio frequency micro-inductors on silicon substrate," *Electron Device Letters, IEEE*, vol. 23, no. 12, pp. 700–703, Dec 2002.

[13] L. Gu and X. Li, "High-Q solenoid inductors with a CMOS-compatible concave-suspending MEMS process," *Microelectromechanical Systems, Journal of*, vol. 16, no. 5, pp. 1162–1172, Oct 2007.

[14] X. Fang, R. Wu, L. Peng, and J. Sin, "A novel silicon-embedded toroidal power inductor with magnetic core," *Electron Device Letters, IEEE*, vol. 34, no. 2, pp. 292–294, Feb 2013.

[15] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture for an LED driver circuit," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 854–861.

[16] M. Araghchini, J. Chen, V. Doan-Nguyen, D. Harburg, D. Jin, J. Kim, M. S. Kim, S. Lim, B. Lu, D. Piedra, J. Qiu, J. Ranson, M. Sun, X. Yu, H. Yun, M. Allen, J. del Alamo, G. DesGroseilliers, F. Herrault, J. Lang, C. Levey, C. Murray, D. Otten, T. Palacios, D. Perreault, and C. Sullivan, "A technology overview of the PowerChip development program," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4182–4201, Sept 2013.

[17] K. Johguchi, T. Hatanaka, K. Ishida, T. Yasufuku, M. Takamiya, T. Sakurai, and K. Takeuchi, "Through-silicon via design for a 3-D solid-state drive system with boost converter in a package," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 269–277, Feb 2011.

[18] K. Zoschke, T. Fischer, M. Topper, K. Samulewicz, O. Wunsch, J. Roder, M. Lutz, O. Ehrmann, and H. Reichl, "Wafer level processing of integrated passive components using polyimide or polybenzoxazole/copper multilayer technology," *Advanced Packaging, IEEE Transactions on*, vol. 33, no. 2, pp. 398–407, May 2010.

[19] H.-H. Lee and J.-Y. Park, "Characterization of fully embedded RF inductors in organic SOP technology," *Advanced Packaging, IEEE Transactions on*, vol. 32, no. 2, pp. 491–496, May 2009.

[20] T. Mori, M. Yamaguchi, S. Kuramochi, and Y. Fukuoka, "Development of a new interposer including embedded thin film passive elements," *Advanced Packaging, IEEE Transactions on*, vol. 32, no. 2, pp. 503–508, May 2009.

[21] S. Mathuna, T. O'Donnell, N. Wang, and K. Rinne, "Magnetics on silicon: an enabling technology for power supply on chip," *Power Electronics, IEEE Transactions on*, vol. 20, no. 3, pp. 585–592, May 2005.

[22] G. Schrom, P. Hazucha, J. Hahn, D. Gardner, B. Bloechel, G. Dermer, S. Narendra, T. Karnik, and V. De, "A 480-MHz, multi-phase interleaved buck DC-DC converter with hysteretic control," in *Power Electronics Specialists Conference (PESC), 2004 IEEE 35th Annual*, vol. 6, June 2004, pp. 4702–4707.

[23] M. Bathily, B. Allard, and F. Hasbani, "A 200-MHz integrated buck converter with resonant gate drivers for an RF power amplifier," *Power Electronics, IEEE Transactions on*, vol. 27, no. 2, pp. 610–613, Feb 2012.

[24] K. Onizuka, K. Inagaki, H. Kawaguchi, M. Takamiya, and T. Sakurai, "Stacked-chip implementation of on-chip buck converter for distributed power supply system in SiPs," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 11, pp. 2404–2410, Nov 2007.

[25] J. Sun, D. Giuliano, S. Devarajan, J.-Q. Lu, T. Chow, and R. Gutmann, "Fully monolithic cellular buck converter design for 3-D power delivery," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 17, no. 3, pp. 447–451, March 2009.

[26] J. Wibben and R. Harjani, "A high efficiency DC-DC converter using 2nH on-chip inductors," in *VLSI Circuits, 2007 IEEE Symposium on*, June 2007, pp. 22–23.

[27] Z. Hayashi, Y. Katayama, M. Edo, and H. Nishio, "High-efficiency DC-DC converter chip size module with integrated soft ferrite," *Magnetics, IEEE Transactions on*, vol. 39, no. 5, pp. 3068–3072, Sept 2003.

[28] H. Bergveld, R. Karadi, and K. Nowak, "An inductive down converter system-in-package for integrated power management in battery-powered applications," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 3335–3341.

[29] S. Lim, J. Ranson, D. Otten, and D. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–12, 2014.

[30] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Applied Power Electronics Conference and Exposition (APEC 2009), Twenty-Fourth Annual IEEE*, Feb 2009, pp. 1–14.

[31] W. Odendaal and J. Ferreira, "Effects of scaling high frequency transformer parameters," in *Industry Applications Conference (IAS '97), Thirty-Second IAS Annual Meeting*, vol. 2, Oct 1997, pp. 1123–1130 vol.2.

[32] W.-J. Gu and R. Liu, "A study of volume and weight vs. frequency for high-frequency transformers," in *Power Electronics Specialists Conference (PESC '93), 24th Annual IEEE*, Jun 1993, pp. 1123–1129.

[33] Coilcraft, *www.coilcraft.com*. Coilcraft, Inc., 2010.

[34] N. Wang, J. Hannon, R. Foley, K. Mccarthy, T. O'Donnell, K. Rodgers, F. Waldron, and C. Mathuna, "Integrated magnetics on silicon for power supply in package (PSiP) and power supply on chip (PwrSoC)," in *Electronic System-Integration Technology Conference (ESTC), 3rd*, Sept 2010, pp. 1–6.

[35] D. Gardner, G. Schrom, P. Hazucha, F. Paillet, T. Karnik, S. Borkar, R. Hallstein, T. Dambrauskas, C. Hill, C. Linde, W. Worwag, R. Baresel, and S. Muthukumar, "Integrated on-chip inductors using magnetic material (invited)," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07E927–07E927–6, Apr 2008.

[36] C. Lei, Y. Zhou, X. Gao, W. Ding, Y. Cao, Z. Zhou, and H. Choi, "Fabrication of 3-D MEMS toroidal microinductor for high temperature application," *Journal of Microelectronics*, pp. 1347–1351, 2006.

[37] D. Lee, K.-P. Hwang, and S. X. Wang, "Design and fabrication of integrated solenoid inductors with magnetic cores," in *Electronic Components and Technology Conference (ECTC 2008), 58th*, May 2008, pp. 701–705.

[38] J.-B. Yoon, B.-K. Kim, C. Han, Y. E., and C. Kim, "Surface micromachined solenoid on-Si and on-glass inductors for RF applications," *Electron Device Letters, IEEE*, vol. 20, no. 9, pp. 487–489, Sept 1999.

[39] M.-H. Chang, K.-H. Lin, J.-W. Huang, and A.-K. Chu, "On-chip solenoid inductors with high quality factor for high frequency magnetic integrated circuits," *Microwave and Wireless Components Letters, IEEE*, vol. 16, no. 4, pp. 203–205, April 2006.

[40] D. Harburg, X. Yu, F. Herrault, C. Levey, M. Allen, and C. Sullivan, "Microfabricated thin-film inductors for on-chip power conversion," in *Integrated Power Electronics Systems (CIPS), 7th International Conference on*, March 2012, pp. 1–6.

[41] R. Wu, J. Sin, and C. Yue, "High-Q backside silicon-embedded inductor for power applications in /spl mu/H and MHz range," *Electron Devices, IEEE Transactions on*, vol. 60, no. 1, pp. 339–345, Jan 2013.

[42] J. Kim, J. Kim, M. Kim, F. Herrault, and M. Allen, "Integrated toroidal inductors with nanolaminated metallic magnetic cores," in *Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS), 13th International Conference on*, Dec 2012, pp. 18–21.

[43] B. Orlando, R. Hida, R. Cuchet, M. Audoin, B. Viala, D. Pellissier-Tanon, X. Gagnard, and P. Ancey, "Low-resistance integrated toroidal inductor for power management," *Magnetics, IEEE Transactions on*, vol. 42, no. 10, pp. 3374–3376, Oct 2006.

[44] C.-H. Ji, F. Herrault, P. Hopper, P. Smeys, P. Johnson, and M. Allen, "Electroplated metal buried interconnect and through-wafer metal-filled via technology for high-power integrated electronics," *Advanced Packaging, IEEE Transactions on*, vol. 32, no. 3, pp. 695–702, Aug 2009.

[45] N. Pham, E. Boellaard, J. Burghartz, and P. Sarro, "Photoresist coating methods for the integration of novel 3-D RF microstructures," *Microelectromechanical Systems, Journal of*, vol. 13, no. 3, pp. 491–499, June 2004.

[46] G. Burger, E. Smulders, J. Berenschot, T. Lammerink, J. Fluitman, and S. Imai, "High resolution shadow mask patterning in deep holes and its application to an electrical wafer feed-through," in *Solid-State Sensors and Actuators and Eurosensors IX (Transducers '95), 8th International Conference on*, vol. 1, Jun 1995, pp. 573–576.

[47] M. Paranjape, F. Giacomozzi, L. Landsberger, M. Kahrizi, B. Margesin, B. Nikpour, and M. Zen, "A micromachined angled hall magnetic field sensor using novel in-cavity patterning," in *Solid State Sensors and Actuators (TRANSDUCERS '97), 9th International Conference on*, vol. 1, Jun 1997, pp. 397–400.

[48] J. Brugger, C. Andreoli, D. M., D. U., H. Rothuizen, and P. Vettiger, "Self-aligned 3D shadow mask technique for patterning deeply recessed surfaces of micro-electro-mechanical systems devices," *Sensors and Actuators A: Physical*, vol. 76, no. 13, pp. 329 – 334, 1999.

[49] S. Morishita, M. Kubota, and Y. Mita, "Integration of EWOD pumping device in deep microfluidic channels using a three-dimensional shadowmask," in *Micro Electro Mechanical Systems (MEMS), IEEE 25th International Conference on*, Jan 2012, pp. 1045–1048.

[50] S. Morishita, J. Kim, F. Marty, Y. Li, A. Walton, and Y. Mita, "A three-dimensional silicon shadowmask for patterning on trenches with vertical walls," in *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS 2009)*, June 2009, pp. 1608–1611.

[51] C. L. Roozeboom, J. Y. Sim, D. Wickeraad, B. Dura, W. S. Smith, M. Hopcroft, P. Hartwell, R. S. Williams, and B. Pruitt, "Multi-functional integrated sensors for the environment," in *Micro Electro Mechanical Systems (MEMS), IEEE 25th International Conference on*, Jan 2012, pp. 144–147.

[52] C. Roozeboom, V. Hong, C. Ahn, E. Ng, Y. Yang, B. Hill, M. Hopcroft, and B. Pruitt, "Multifunctional integrated sensor in a 2x2 mm epitaxial sealed

chip operating in a wireless sensor node," in *Micro Electro Mechanical Systems (MEMS), 2014 IEEE 27th International Conference on*, Jan 2014, pp. 773–776.

[53] F. Herrault, B. Yen, C.-H. Ji, Z. Spakovszky, J. H. Lang, and M. Allen, "Fabrication and performance of silicon-embedded permanent-magnet microgenerators," *Microelectromechanical Systems, Journal of*, vol. 19, no. 1, pp. 4–13, Feb 2010.

[54] X. Yu, M. Kim, F. Herrault, J. C-H., J. Kim, and M. Allen, "Silicon-embedded 3D toroidal air-core inductor with through-wafer interconnect for on-chip integration," in *Micro Electro Mechanical Systems (MEMS), 2012 IEEE 25th International Conference on*, Jan 2012, pp. 325–328.

[55] C. Chung and M. Allen, "Uncrosslinked SU-8 as a sacrificial material," *Journal of Micromechanics and Microengineering*, vol. 15, no. 1, p. N1, 2005.

[56] C. Sullivan, "Integrating magnetics for on-chip power: Challenges and opportunities," in *Custom Integrated Circuits Conference (CICC '09), IEEE*, Sept 2009, pp. 291–298.

[57] C. Sullivan, W. Li, S. Prabhakaran, and S. Lu, "Design and fabrication of low-loss toroidal air-core inductors," in *Power Electronics Specialists Conference (PESC 2007), IEEE*, June 2007, pp. 1754–1759.

[58] J. Hannon, R. Foley, J. Griffiths, D. O'Sullivan, K. McCarthy, and M. Egan, "A 20 MHz 200-500 mA monolithic buck converter for RF applications," in *Applied Power Electronics Conference and Exposition(APEC), 24th Annual IEEE*, Feb 2009, pp. 503–508.

[59] X. Yu, J. Kim, F. Herrault, and M. Allen, "Silicon-embedded toroidal inductors with magnetic cores: Design methodology and experimental validation," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, March 2014, pp. 763–767.

[60] M. Araghchini and J. Lang, "Modeling, design and performance of integrated power electronics using MEMS toroidal inductors," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, March 2014, pp. 519–526.

[61] Y. Han and D. Perreault, "Inductor design methods with low-permeability RF core materials," *Industry Applications, IEEE Transactions on*, vol. 48, no. 5, pp. 1616–1627, Sept 2012.

[62] W. Kuhn and N. Yanduru, "Spiral inductor substrate loss modeling in silicon RF ICs," in *Radio and Wireless Conference (RAWCON 98)*, Aug 1998, pp. 305–308.

[63] C. Yue and S. Wong, "A study on substrate effects of silicon-based RF passive components," in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 4, June 1999, pp. 1625–1628.

[64] P. Dowell, "Effects of eddy currents in transformer windings," *Electrical Engineers, Proceedings of the Institution of*, vol. 113, no. 8, pp. 1387–1394, August 1966.

[65] K. W. E. Cheng and P. Evans, "Calculation of winding losses in high-frequency toroidal inductors using single strand conductors," *Electric Power Applications, IEE Proceedings*, vol. 141, no. 2, pp. 52–62, Mar 1994.

[66] A. Reatti and M. Kazimierczuk, "Comparison of various methods for calculating the AC resistance of inductors," *Magnetics, IEEE Transactions on*, vol. 38, no. 3, pp. 1512–1518, May 2002.

[67] M. Araghchini, X. Yu, M. Kim, J. Qiu, F. Herrault, C. Sullivan, M. Allen, and J. Lang, "Modeling and measured verification of stored energy and loss in MEMS toroidal inductors," *Industry Applications, IEEE Transactions on*, vol. 50, no. 3, pp. 2029–2038, May 2014.

[68] C. Yue, C. Ryu, J. Lau, T. Lee, and S. Wong, "A physical model for planar spiral inductors on silicon," in *Electron Devices Meeting (IEDM '96), International*, Dec 1996, pp. 155–158.

[69] C. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 5, pp. 743–752, May 1998.

[70] M. Araghchini, J. Lang, X. Yu, M. S. Kim, F. Herrault, M. Allen, J. Qiu, and C. Sullivan, "Modeling and measured verification of stored energy and loss in MEMS toroidal inductors," in *Energy Conversion Congress and Exposition (ECCE)*, Sept 2012, pp. 3293–3300.

[71] K. W. E. Cheng and P. Evans, "Calculation of winding losses in high frequency toroidal inductors using multistrand conductors," *Electric Power Applications, IEE Proceedings* -, vol. 142, no. 5, pp. 313–322, Sep 1995.

[72] X. Yu, M. Araghchini, F. Herrault, J. Kim, and M. Allen, "Fabrication, modeling and performance analysis of silicon-embedded 3-d toroidal inductors," in *PowerMEMS, 2012*, Dec 2012, pp. 763–767.

[73] Y. Han, G. Cheung, A. Li, C. Sullivan, and D. Perreault, "Evaluation of magnetic materials for very high frequency power applications," *Power Electronics, IEEE Transactions on*, vol. 27, no. 1, pp. 425–435, Jan 2012.

[74] Micrometals, *RF Applications, Issue H.* Micrometals, INC., 2005.

[75] J. Kim, F. Herrault, X. Yu, M. Kim, R. H. Shafer, and M. Allen, "Microfabrication of air core power inductors with metal-encapsulated polymer vias," *Journal of Micromechanics and Microengineering*, vol. 23, no. 3, pp. 1–7, March 2013.

[76] National Magnetics Group, *http://www.magneticsgroup.com.* National Magnetics Group—TCI Ceramics, 2014.

[77] Fair-Rite, *http://www.fair-rite.com/newfair/index.htm.* Fair-Rite Products Corp., 2014.

[78] J. Qiu, *Thin-Film Inductors for Multi-Megahertz Power Conversion.* Dartmouth College, 2013.

[79] J. Qiu and C. Sullivan, "Radial-anisotropy nanogranular thin-film magnetic material for toroidal inductors," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, Feb 2012, pp. 491–497.

[80] J. Qiu, H. Syed, and C. Sullivan, "Complex permeability measurements of radial-anisotropy thin-film magnetic toroidal cores," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 628–634.

[81] J. Qiu, A. Hanson, and C. Sullivan, "Design of toroidal inductors with multiple parallel foil windings," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, June 2013, pp. 1–6.

[82] J. Qiu, D. Harburg, and C. Sullivan, "A toroidal power inductor using radial-anisotropy thin-film magnetic material based on a hybrid fabrication process," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 1660–1667.

[83] S. Hui and W. Ho, "A new generation of universal contactless battery charging platform for portable consumer electronic equipment," *Power Electronics, IEEE Transactions on*, vol. 20, no. 3, pp. 620–627, May 2005.

[84] C. Sonntag, E. Lomonova, J. Duarte, and A. J. A. Vandenput, "Specialized receivers for three-phase contactless energy transfer desktop applications," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–11.

[85] G. Wang, W. Liu, M. Sivaprakasam, and G. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 10, pp. 2109–2117, Oct 2005.

[86] R. Selvakumaran, W. Liu, B. Soong, L. Ming, and S. Y. Loon, "Design of inductive coil for wireless power transfer," in *Advanced Intelligent Mechatronics (AIM 2009), IEEE/ASME International Conference on*, July 2009, pp. 584–589.

[87] P. Meyer, P. Germano, M. Markovic, and Y. Perriard, "Design of a contactless energy transfer system for desktop peripherals," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, Sept 2010, pp. 2253–2258.

[88] WiTricity, *http://www.witricity.com.* WiTricity Corp., 2014.

[89] J. de Boeij, E. Lomonova, and A. Vandenput, "Contactless energy transfer to a moving load part I: Topology synthesis and FEM simulation," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2, July 2006, pp. 739–744.

[90] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 10, pp. 1419–1424, Oct 1999.

[91] C. Yue and S. Wong, "Physical modeling of spiral inductors on silicon," *Electron Devices, IEEE Transactions on*, vol. 47, no. 3, pp. 560–568, Mar 2000.

[92] Y.-Q. Hu, D.-W. Cheng, and Y. S. Lee, "New fabrication method for planar multilayer windings used in low-profile magnetic components," *Magnetics, IEEE Transactions on*, vol. 35, no. 2, pp. 1055–1059, Mar 1999.

[93] W. Kuhn and N. Ibrahim, "Analysis of current crowding effects in multiturn spiral inductors," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 1, pp. 31–38, Jan 2001.

[94] P. Scholz, C. Reinhold, W. John, and U. Hilleringmann, "Analysis of energy transmission for inductive coupled RFID tags," in *RFID, IEEE International Conference on*, March 2007, pp. 183–190.

[95] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification.* John Wiley and Sons, 2003.

[96] Y. Lee, *Antenna Circuit Design Application Note AN710.* Microchip technologies, 2003.

[97] J. Kim, M. Kim, F. Herrault, J. Park, and M. Allen, "Highly laminated soft magnetic electroplated CoNiFe thick films," *Magnetics Letters, IEEE*, vol. 4, pp. 5 000 204–5 000 204, 2013.